

Caliber Interconnect Solutions

Design For Perfection

ATE Design Capabilities



Load boards: Probe cards: PIB: Daughter Cards: Evaluation/Bench Boards: FPCB

Caliber Interconnect Solutions (Pvt)Ltd No 9 B/1, Poombukar Nagar, Thudiyalur, Coimbatore-641034. Tamil Nadu, India. www.caliberinterconnect.com

MISSION & VISION

"Provide dependable solutions to the satisfaction of the customers through intensive R&D and proven quality control procedures using disciplined workforce."

MISSION

VISION

"Developing and applying technological solutions to the benefits of the society that will not affect the safety and living standards of our future generations"

QUALITY POLICY "CALIBER INTERCONNECT SOLUTIONS
PRIVATE LIMITED

Is committed to meet and exceed customers expectations through timely delivery of cost effective quality designs through ever improving process and team work."

SERVICES

ATE test interface board design services

MLC / MLO substrate design services

HSD & HDI design services

Signal & Power Integrity simulation and optimization

Library development and maintenance

CAM validation and editing

STRUCTURE

Caliber is known for its Quality and Quick Turn arounds.

Exclusive teams for Library, ATE routing, Signal Integrity, Quality control, CAM validation and inhouse software development enables high quality and quick deliveries.

Signal Routing Library Integrity Fleet **DESIGN** Quality CAM Software **Validation** Control

Team

Caliber's Design Process is controlled and certified. It empowers each and every individual in the organization to deliver consistently and effectively.

WE WORK CLOSE WITH

Integrated C i r c u i t (IC)Design Houses and Fabricators Test Houses and Socket manufacturers

Probe vendors and assemblers

Test Interface board fabricators and Design houses

Caliber's ATE Board Design Services

EXPERTISE

Versatile in interface and HSD

:: DDR :: USB :: PCle::

:: SATA :: HDMI :: LVDs ::

:: SerDes ::

:: Till 12Gbps is Usual handling ::

Fine/Coarse DFM handling

:: 0.4mmpitch ::

:: micro via(blind & buried) ::

:: Hybrid stack-ups ::

:: Designed max 52 layers in 6.35mm::

:: Done 64 layers maximum ::

Design Expertise

Electrical knowledge

::Mixed signal::

::Mixed impedance design(50/90/100 Ohms)::

::Mixed topology (Star ,chain, tree ...)::

::Skilful in Shield/Tuning/Force & Sense::

Experience

::15 years in ATE interface brd design::

:: Delivered 7500+ designs::

:: Multiple EDA tool knowledge::

:: auto-tools and skills for ATE routing::

ATE BOARD TYPES

Loadboards (Final test)



Probe Interface Boards (PIB orWS)



Probe cards

Vertical Po

Vertical PC (conventional and direct docking) Cantilever PC (conventional and direct docking)



Spider cards

FPCB



05

Daughter cards



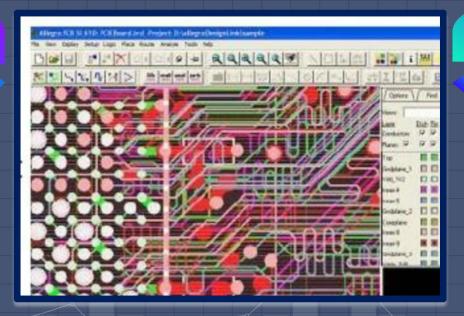
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(sub boards to enable HSD in existing PC)



TESTER PLATFORMS

- ETS
- IntegraFlex
- J750 (EX)
- LTX Fusion
- MicroFlex
- Nextest
- Sapphire
- ST6730
- UltraFlex
- VLCT



- 93K
- T6577
- T6575
- T6371/72/73
- T2000
- AL9740
- Catalyst
- D10
- DiamondX

Caliber is expertise in a wide variety of ATE platforms

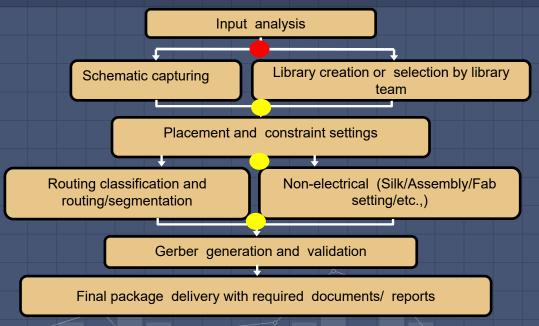
Frequently used Instrument types

...but not limited to

Advantest Platform	Teradyne Platform
PSI600/800/400	UPI600/800
GPDPS	HSD1000
MSDPS	HexVS
UHCSUPPLY	HDVS
9G	DCIO
VI32	US10G
DPS32	DC30
AWG	DC75
HSIF	DC90
RVS	APU
UDC	SPO
LCD IO	СТО

Caliber's Design Flow for ATE

The below is the conventional flow of Caliber for ATE designs. More opt procedures can be adopted and tailored based on customer needs.



- 1. Stage-wise QA will be done at this points. Also final QA will be done at final stage.
- 2. After that the files will be sent to customer for review and stage wise approval
- 3. After initial input analysis, any data insufficiency will be reported at this point
 - Template choosing/creating and approval will be initiated in this stage and will be completed before placement stage

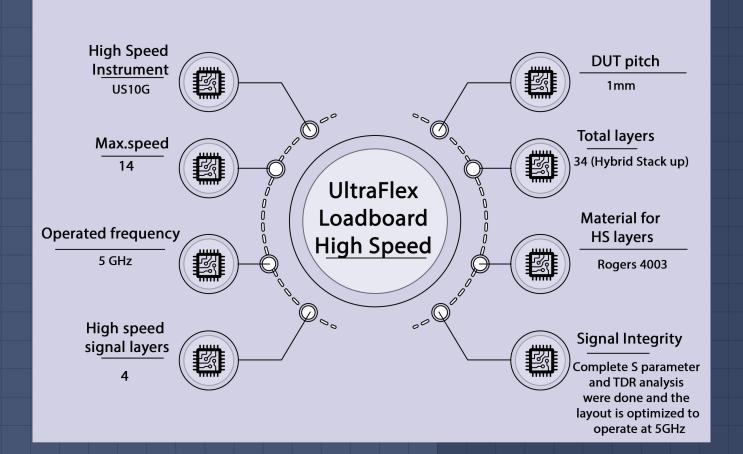
Design with Signal Integrity

Caliber have in-house SI team powered by latest state-of-art simulation tools like Ansys and Sigrity.

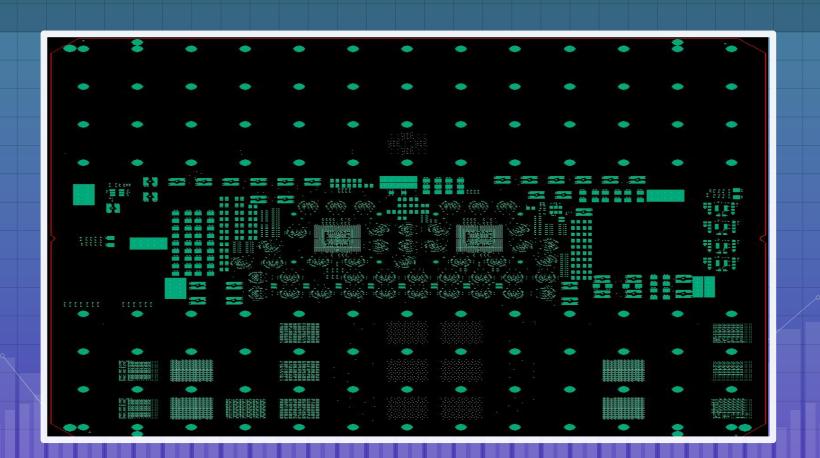
This enables Caliber to implement high speed testing interfaces in the designs more effectively.

The following slides will detail such an example.

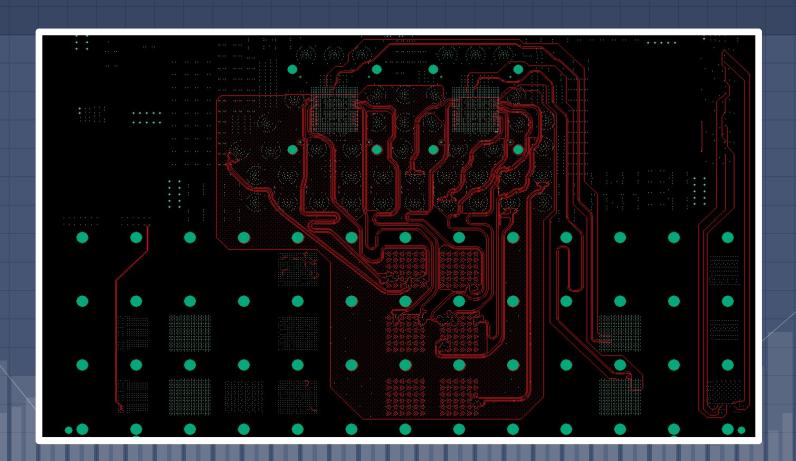
1. UltraFlex Loadboard - High Speed



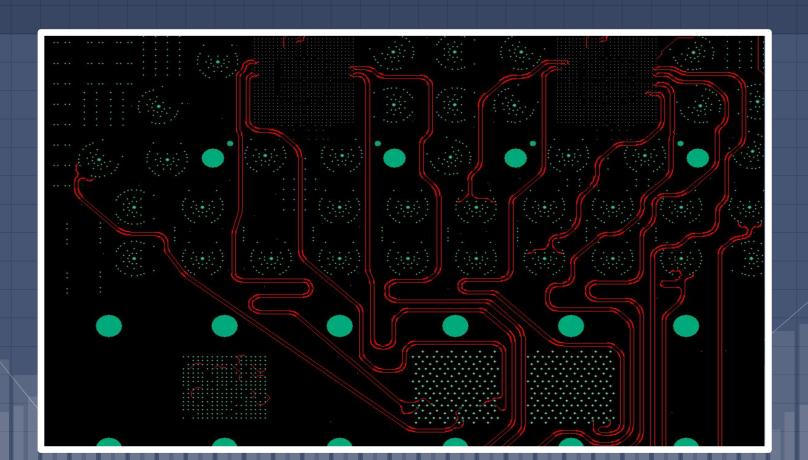
Component placement view



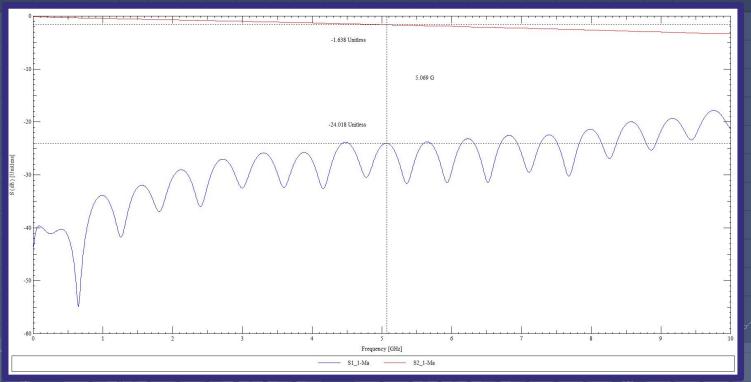
High Speed Signal Layer



Closer look of Routing



S-parameters measurement after optimization



Given for one sample TX channel here, this result is taken after optimizing the layout from Initial SI feedback

Probe card Expertise

Substrate to PIB:

Logic & Memory:

New Templates & PIB:

Substrate (MLO/MLC)designs, Probe card designs and Probe Interface Board (PIB/WS) designs under a single roof.

Vast experience in both Logic and Memory devices(wafers).

On the reception of Mapping & Mechanical, Template creation for new tester platforms or template creation for customized PIB

Probe card Expertise

SPL:

Support boards:

Mixed Signal:

Layer composition:

Complex CPC-SPL pattern creation for over 3000 pins in a single day. Easy to solder reserves of unused IO/Power.

Daughter card and FPCB design to facilitate support/reusage of Universal Probe cards.

Multiple GND designs(mixed signal) for perfect Noise Isolation.

Stack up proposal along with impedance simulations. Symmetrical and balanced design. Hybrid stack ups with different dielectrics to handle High Speed.

Probe card –Usual cases

Most commonly facing scenarios

CPC,VPC and Direct Docking cases

Power count ranging from 12 to 256

MUX and Relay circuitry

Layers in range of 14 to 48 (impedance controlled boards)

IO count ranging from 512 to 2500

Maximum components:2812 in Direct Docking

Customized PIB template creation

Maximum of 10256 IO/ Sense lines;1528 power shapes in memory probe cards

Thickness range of 4.5mm to 6.35mm

Analog signal on ATE

In-depth knowledge in handling Analog Layout

High bandwidth Analog signals

Shielding preferences

Low amplitude signals

Gnd reference by splits and shorts

Mixed layout for digital & Analog

EDA to ATE Router (To Plan and Route)



[Allegro/Expedition/Cadvance/Pads andothers]

Transferred through

Internally developed Software

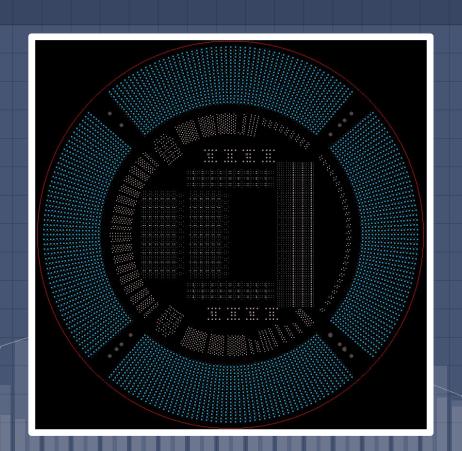
ATE

Router
[The design is divided into multiple modules and thus multiple resources can work and reduce the time to delivery]

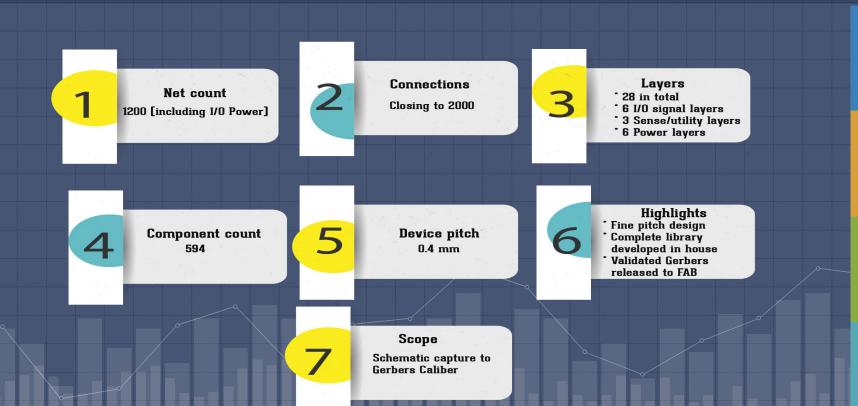
DXF or ASCII files

Following slides will give a closer look on the recently done Probecard designs

High pin count SPL/Reserve for CPC



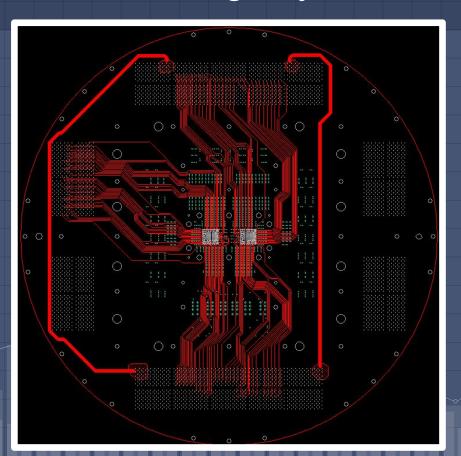
Ultra Flex Probe card (0.4mm pitch :VPC)



Component placement view



Routing Layer



J750 Probe card (CPC)



Component placement view



Inner layer routing image

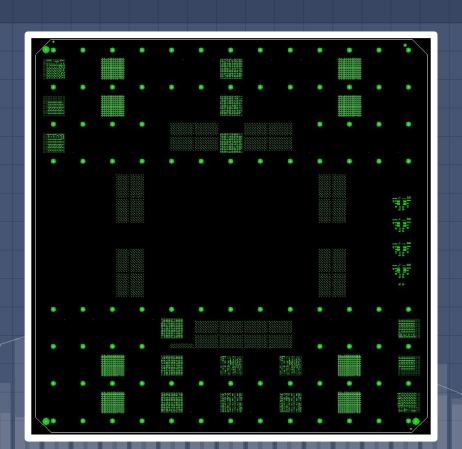


Following slides will give a closer look on the recently done PIB designs

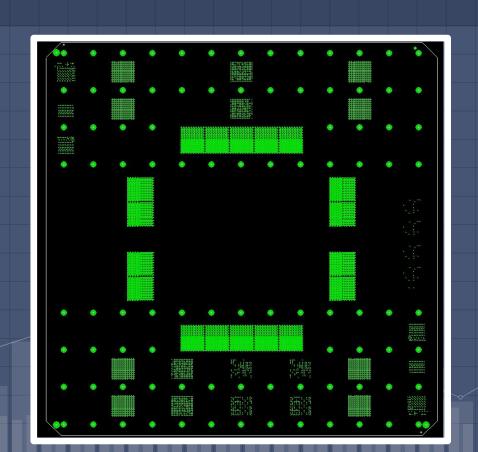
1. Ultra Flex PIB

Component Scope **Net count** Layers Highlights count * Complete library * 28 in total 1900 [including developed in house Schematic capture * 6 I/O signal layers I/O Power] * Validated Gerbers to Gerbers * 2 Utility layers released for FAB * 6 Power layers * Blind vias used at POGO interface area 05 02 01

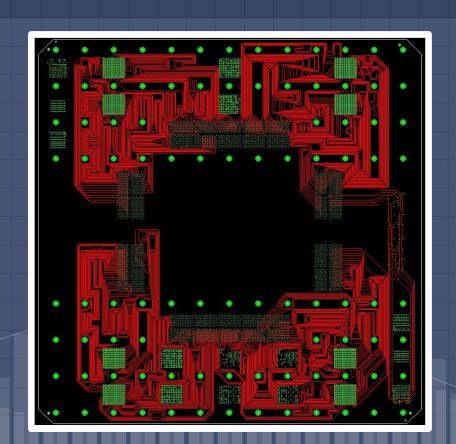
Top view



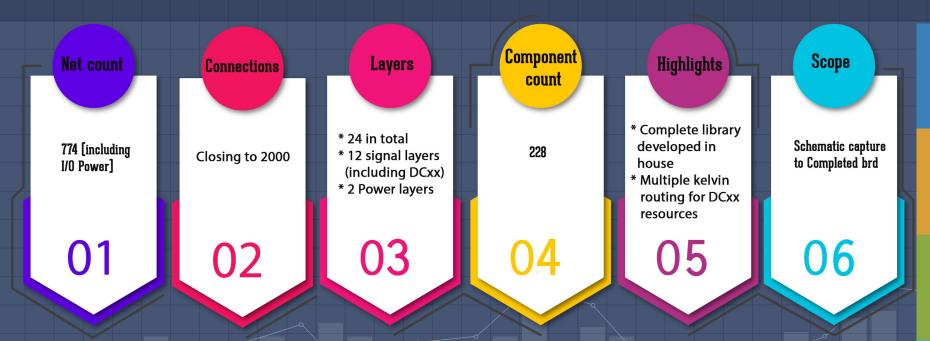
Bottom view



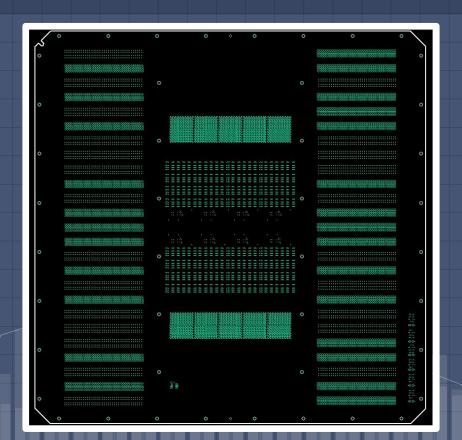
Signal Layer



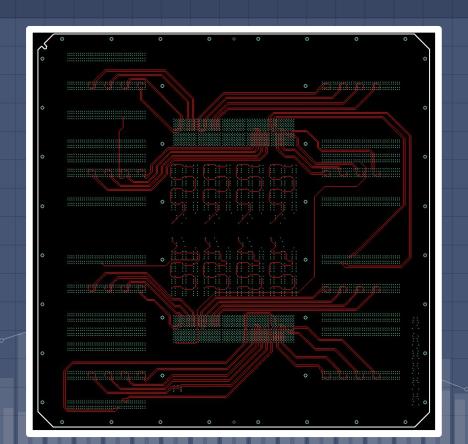
2. Integra FLEX PIB



Component Placement View



DC xx Resource Routing



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THANK YOU

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