



Caliber Interconnect Solutions

Design for perfection

Samples from our ATE Design Database

Caliber Interconnect Solutions (Pvt) Ltd
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Loadboards

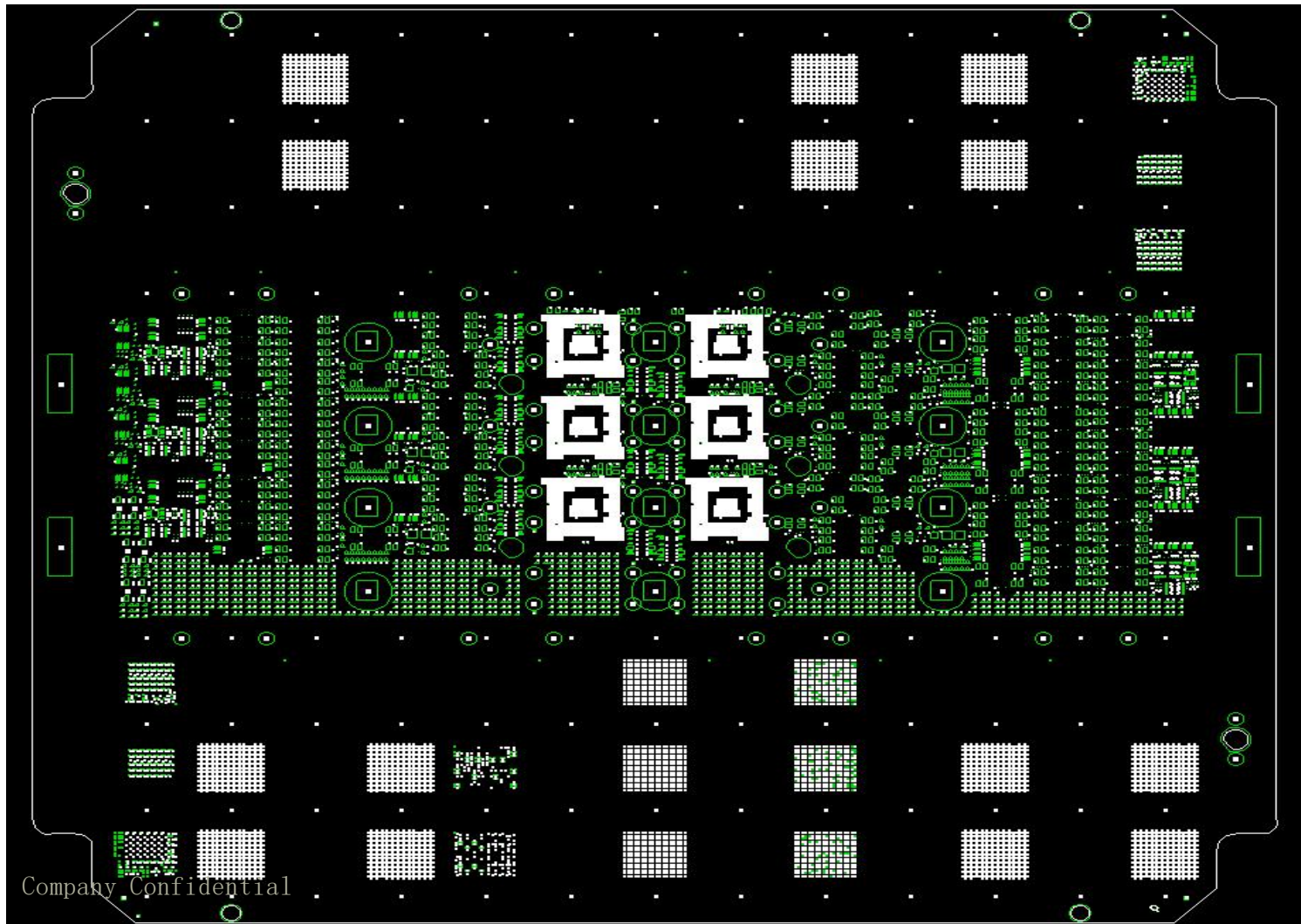


1. UltraFlex Loadboard

- ⌘ **Net count** : 3013 (including I/O & Power)
- ⌘ **Connections** : closing to 8000
- ⌘ **Layers** : 56 in total
 - ⌘ 13 I/O signal layers
 - ⌘ 4 UVS256 layers
 - ⌘ 8 VI80 layers
- ⌘ **Component count** : 1850
- ⌘ **DUT pitch** : 1mm
- ⌘ **Highlights** :
 - ⌘ Perfectly optimized power plane design
 - ⌘ Highly optimized routing with perfect tuning/spacing
- ⌘ **Scope** : Schematic capture to completed brd
- ⌘ **Timeline** : 15 days (includes: Schematic capture to Layout completion
excludes : Customer review days)

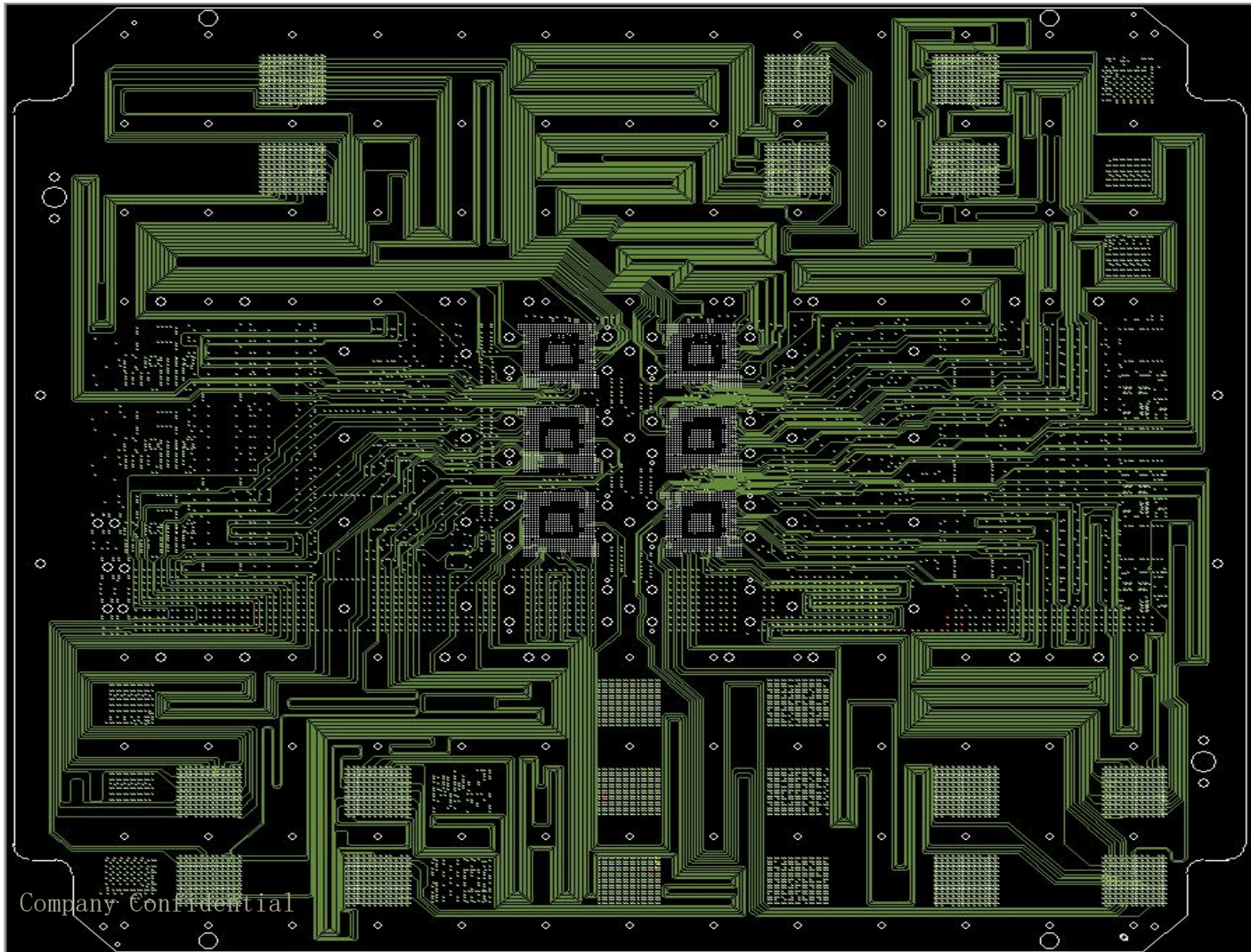


Component placement view





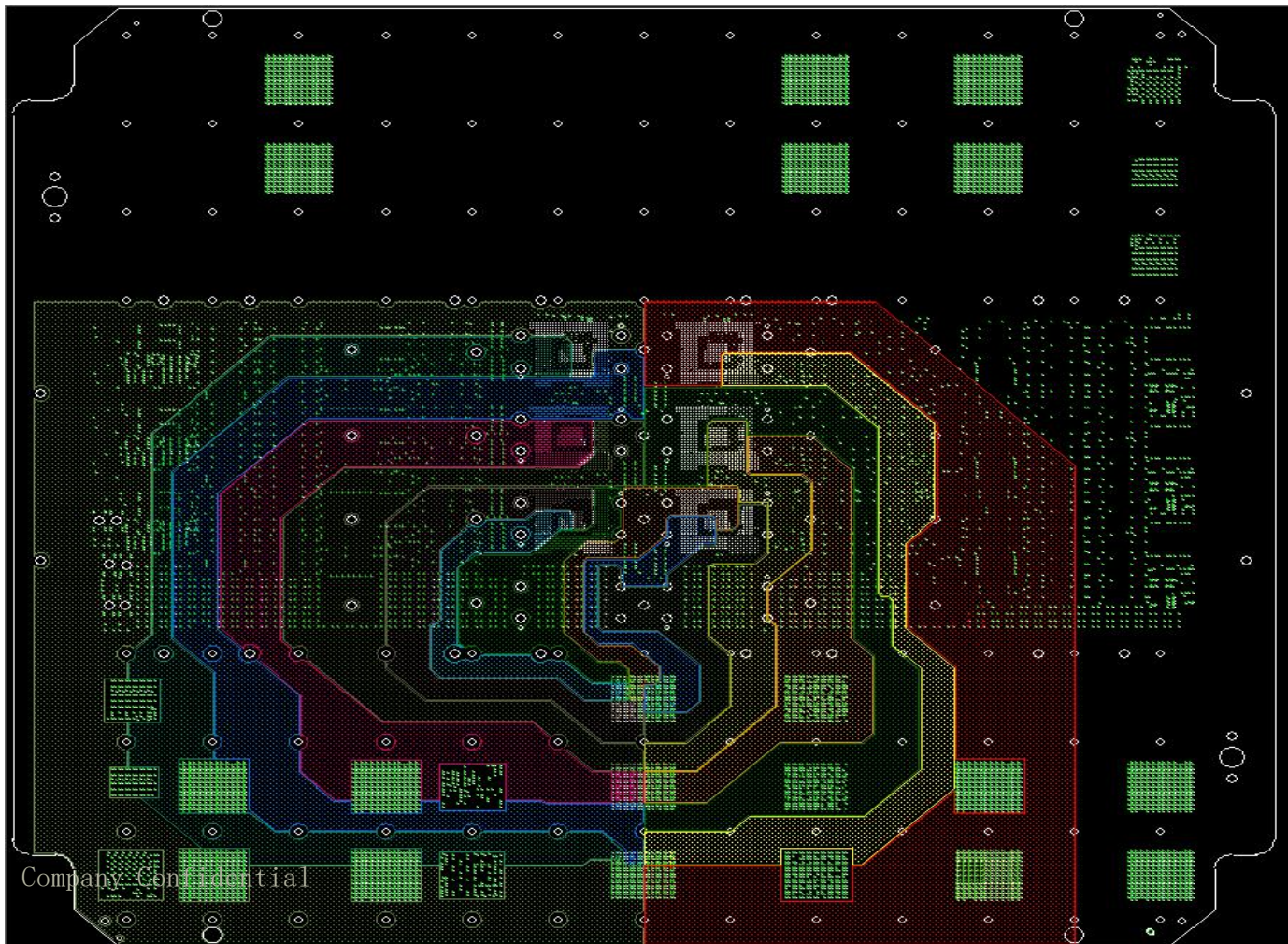
Routing layer



Company Confidential



Optimized power shapes



Company Confidential

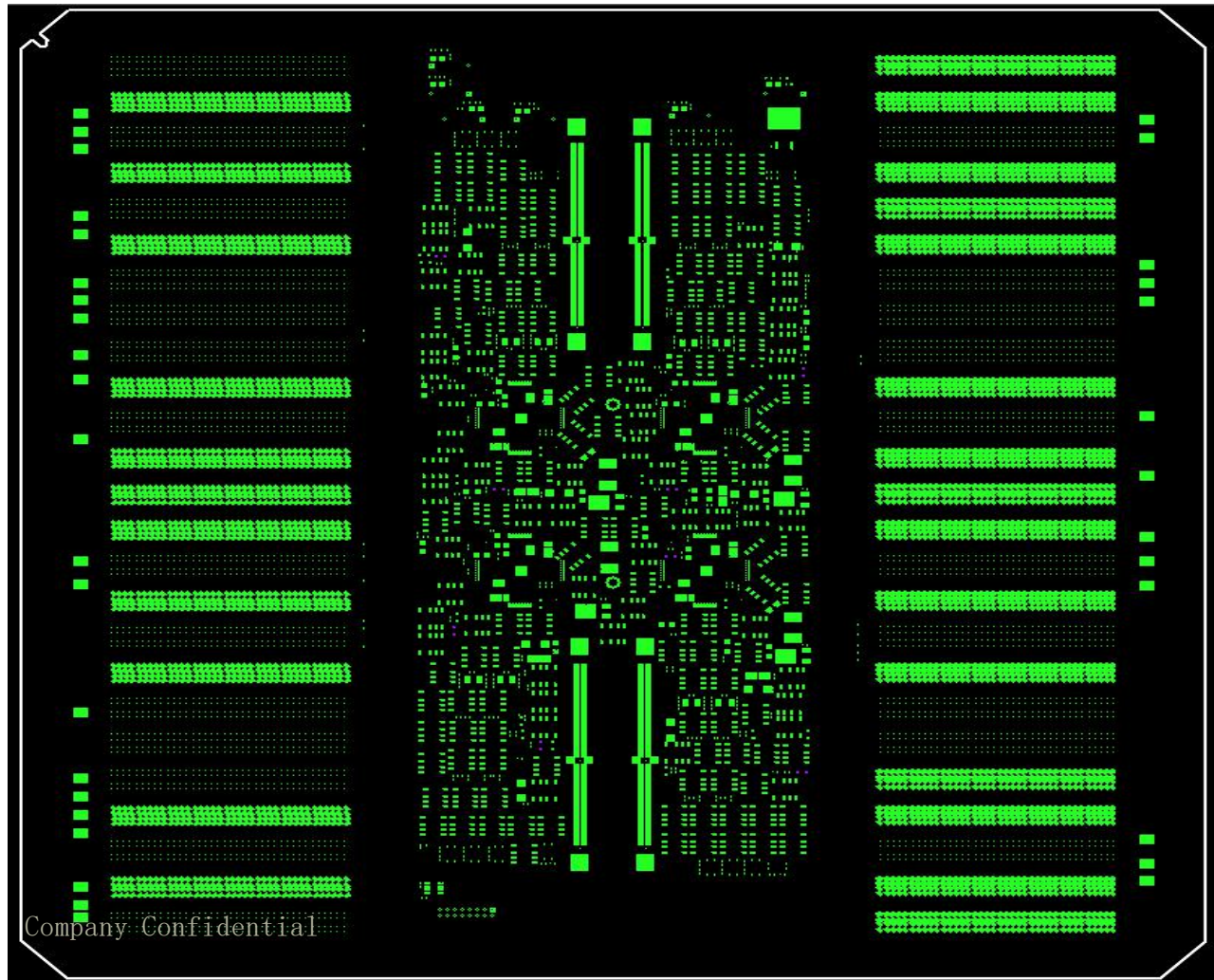


2. IntegraFLEX Loadboard

- ⌘ Net count : 1087 (including I/O & Power)
- ⌘ Connections : closing to 4500
- ⌘ Layers : 28 in total
 - ⌘ 8 I/O signal layers
 - ⌘ 9 Power layers
- ⌘ Component count : 629
- ⌘ DUT pitch : 1mm
- ⌘ Highlights :
 - ⌘ Switching of I/O and DC through multiple circuits
 - ⌘ Kelvin routing to DUT pins to source multiple type resources
- ⌘ Scope : Schematic capture to completed brd
- ⌘ Timeline : 9 days (include: Schematic capture to Layout completion)



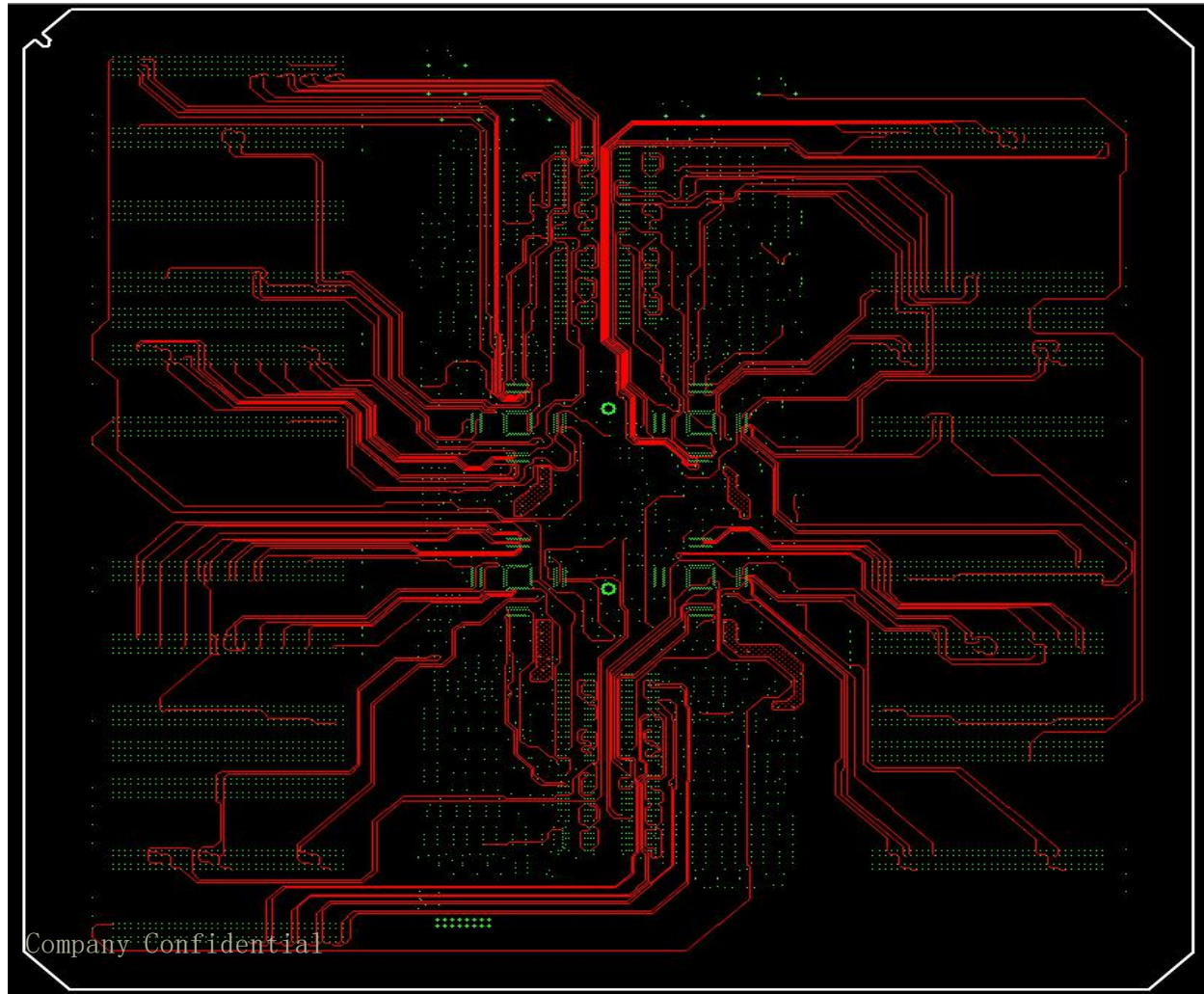
Component placement view



Company Confidential



Inner layer routing image



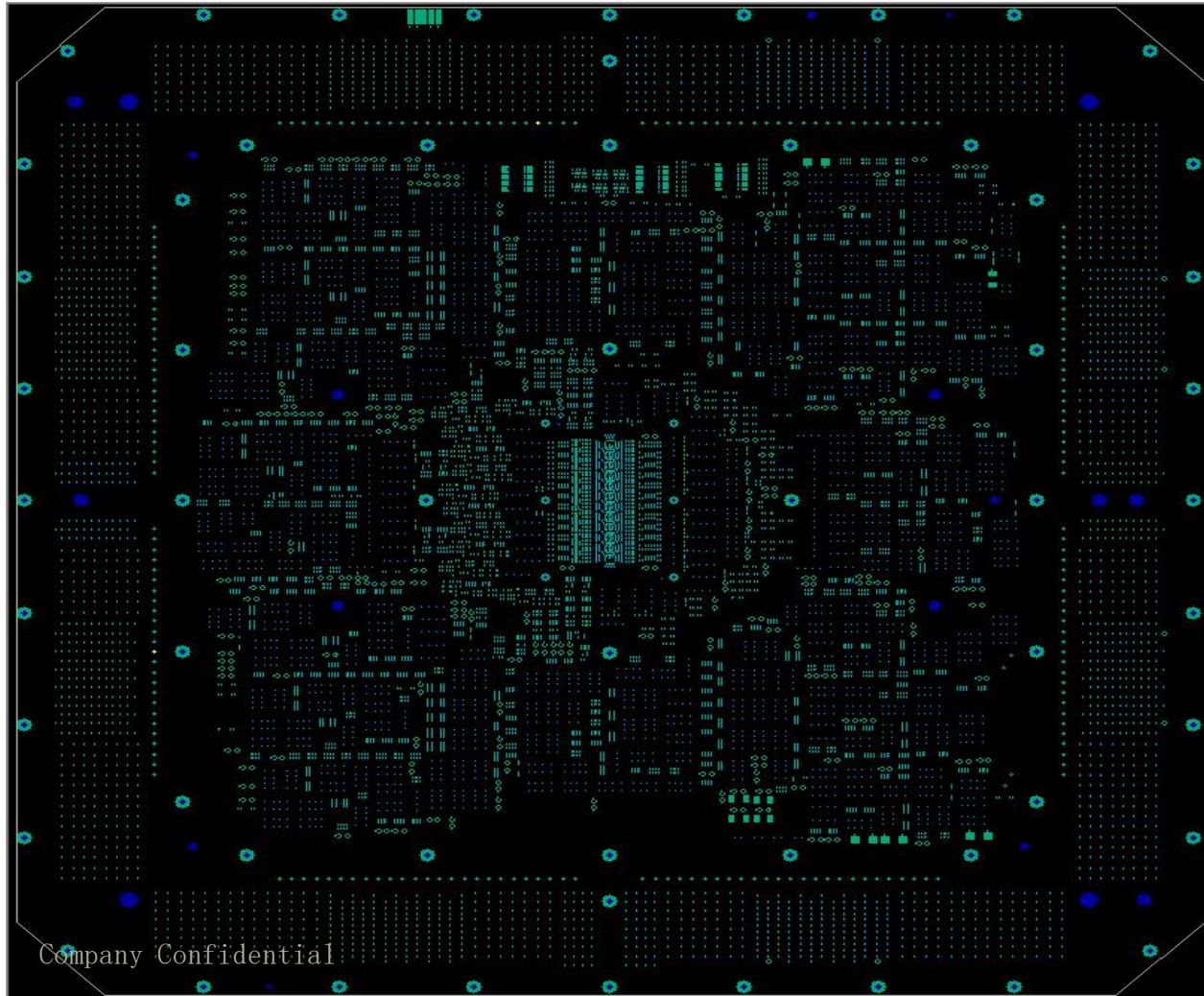


3. ETS364 Loadboard

- ⌘ Net count : 1347 (including I/O & Power)
- ⌘ Connections : closing to 4000
- ⌘ Layers : 44 in total
 - ⌘ 24 I/O signal layers (rest is Pwr/Gnd)
- ⌘ Component count : 1683
- ⌘ DUT pitch : 0.4 mm
- ⌘ Highlights :
 - ⌘ High component count
 - ⌘ Densely placed vias made routing more challenging
- ⌘ Scope : Placement to completed brd
- ⌘ Timeline : 6 days (includes: Layout only)

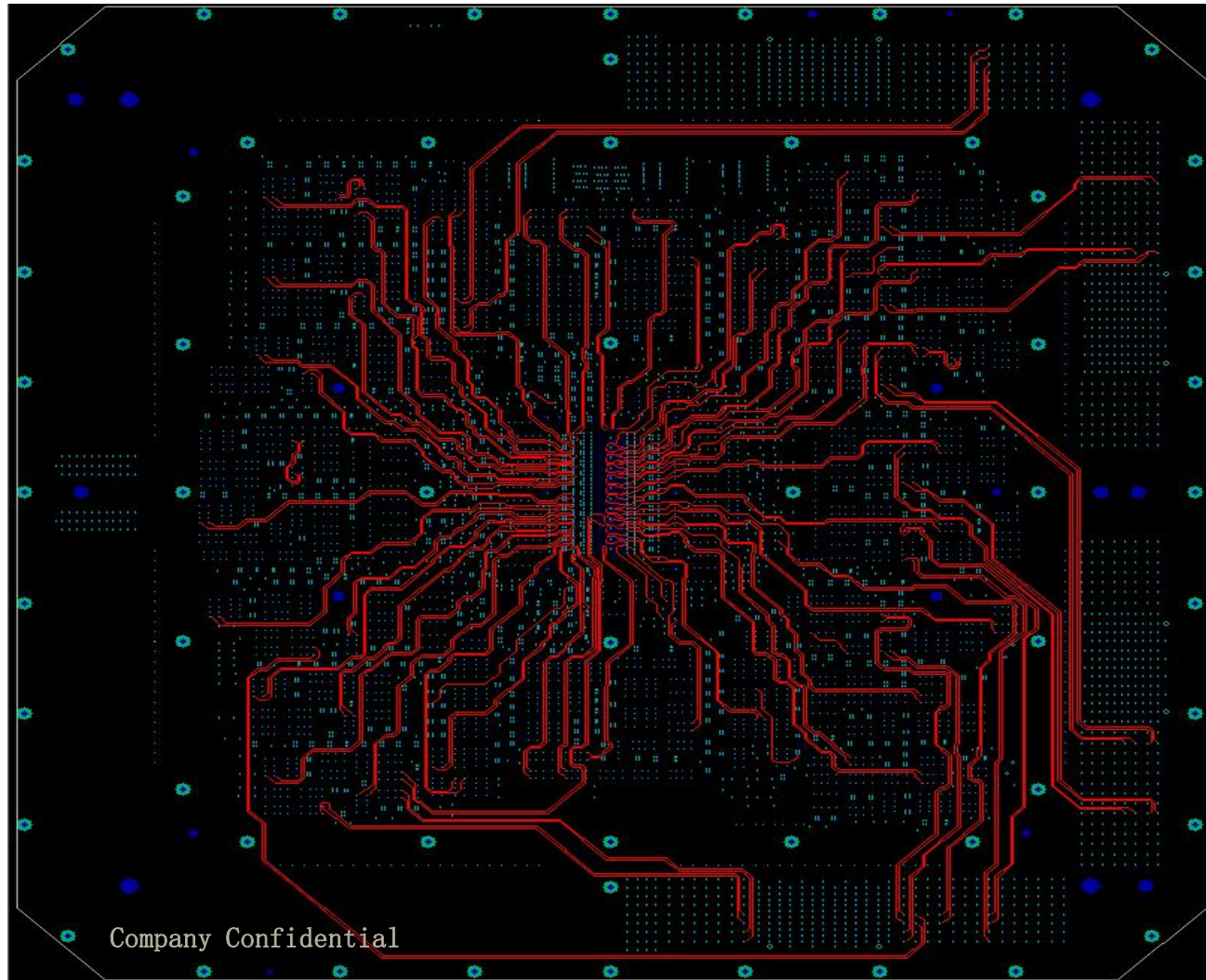


Component placement view





Inner layer routing image



Company Confidential

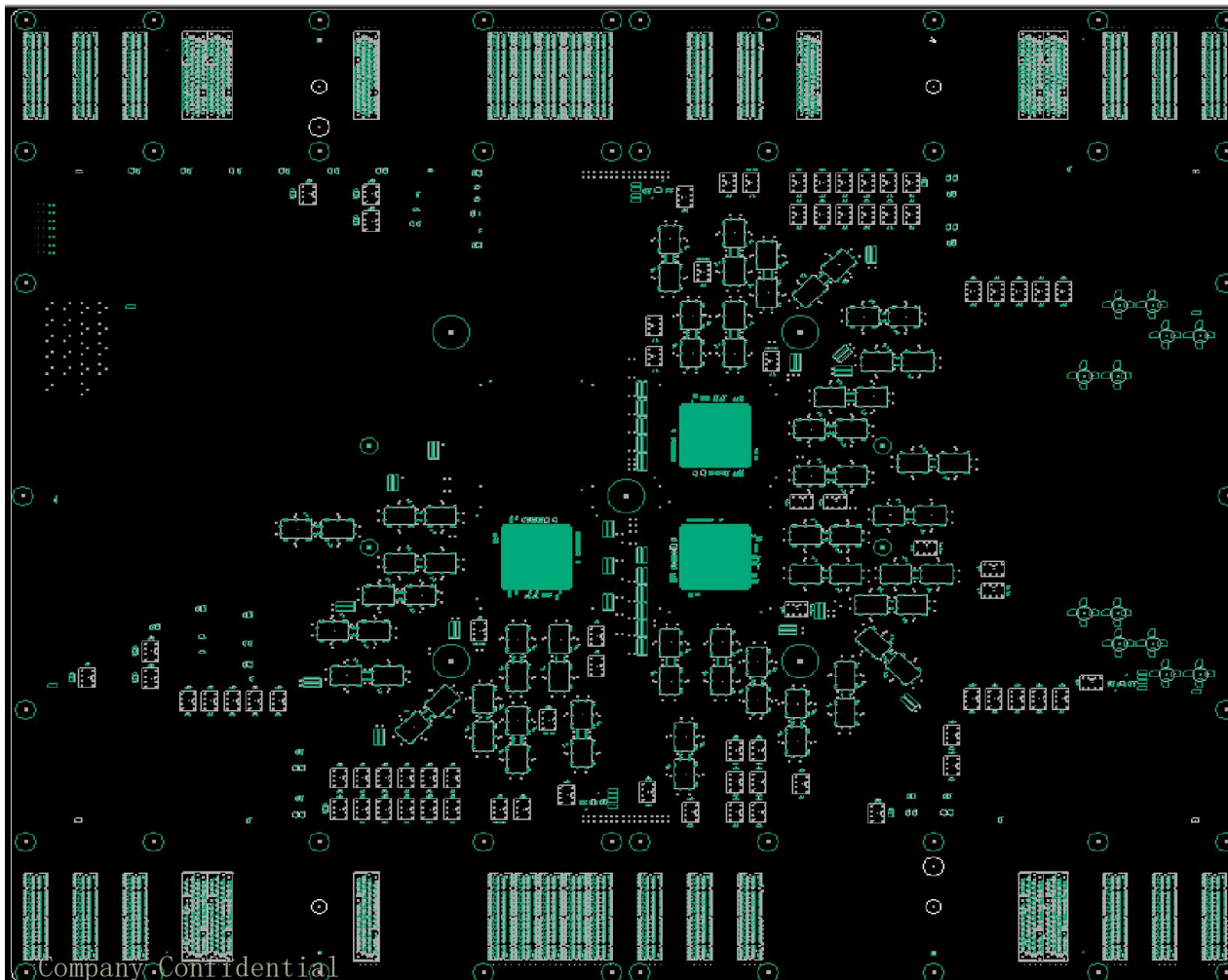


4.T2000 Loadboard

- ⌘ Net count : 2710 (including I/O & Power)
- ⌘ Connections : closing to 11300
- ⌘ Layers : 32 in total
 - ⌘ 14 I/O signal layers
 - ⌘ 4 Power layers
- ⌘ Component count : 1280
- ⌘ DUT pitch : 1mm
- ⌘ Highlights :
 - ⌘ Similar routing and performance on all 3 SITEs
- ⌘ Scope : Schematic capture to completed brd
- ⌘ Timeline : 8 days (includes: Schematic capture to Layout completion
excludes : Customer review days)

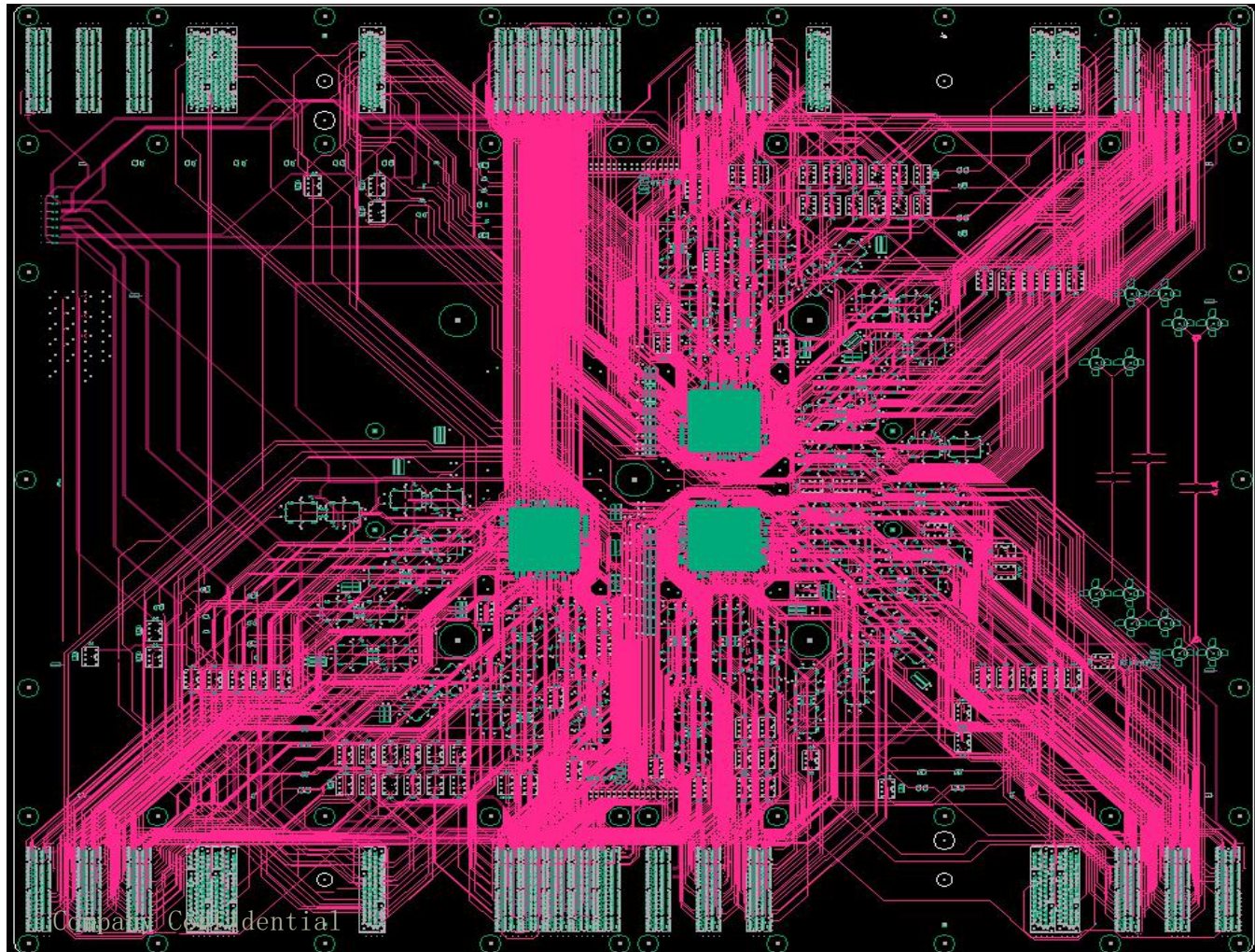


Placement Image





Routing layer (overall)



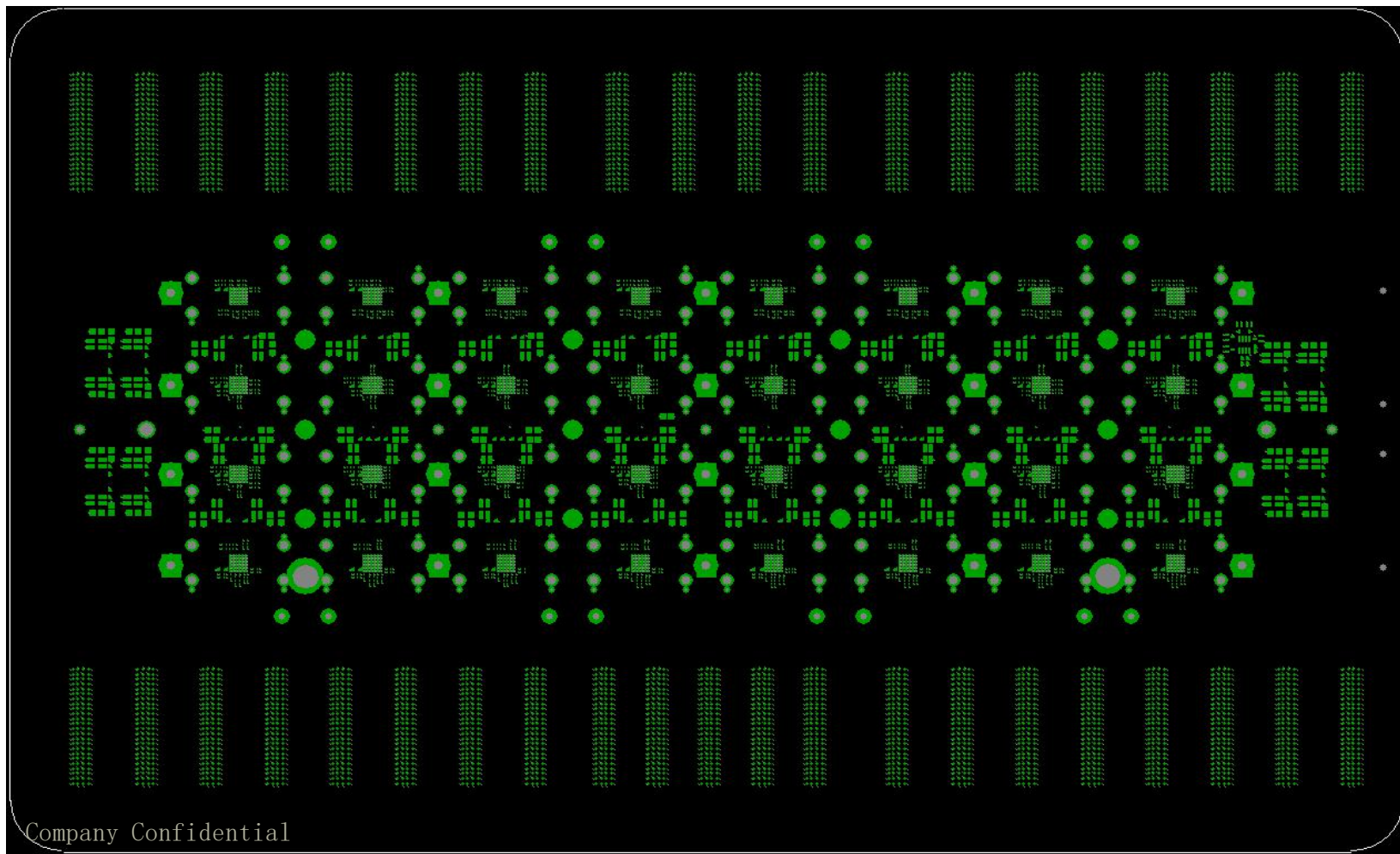


5. J750 Loadboard

- ⌘ Net count : 1366 (including I/O & Power)
- ⌘ Connections : closing to 3000
- ⌘ Layers : 28 in total
 - ⌘ 4 I/O signal layers
 - ⌘ 6 HDDPS layers
 - ⌘ 2 CTO layers
- ⌘ Component count : 819
- ⌘ DUT pitch : 0.65 mm
- ⌘ Highlights :
 - ⌘ Complete library developed in-house
 - ⌘ Highly optimized routing with perfect tuning/spacing
- ⌘ Scope : Schematic capture to completed brd
- ⌘ Timeline : 9 days (includes: Schematic capture to Layout completion)

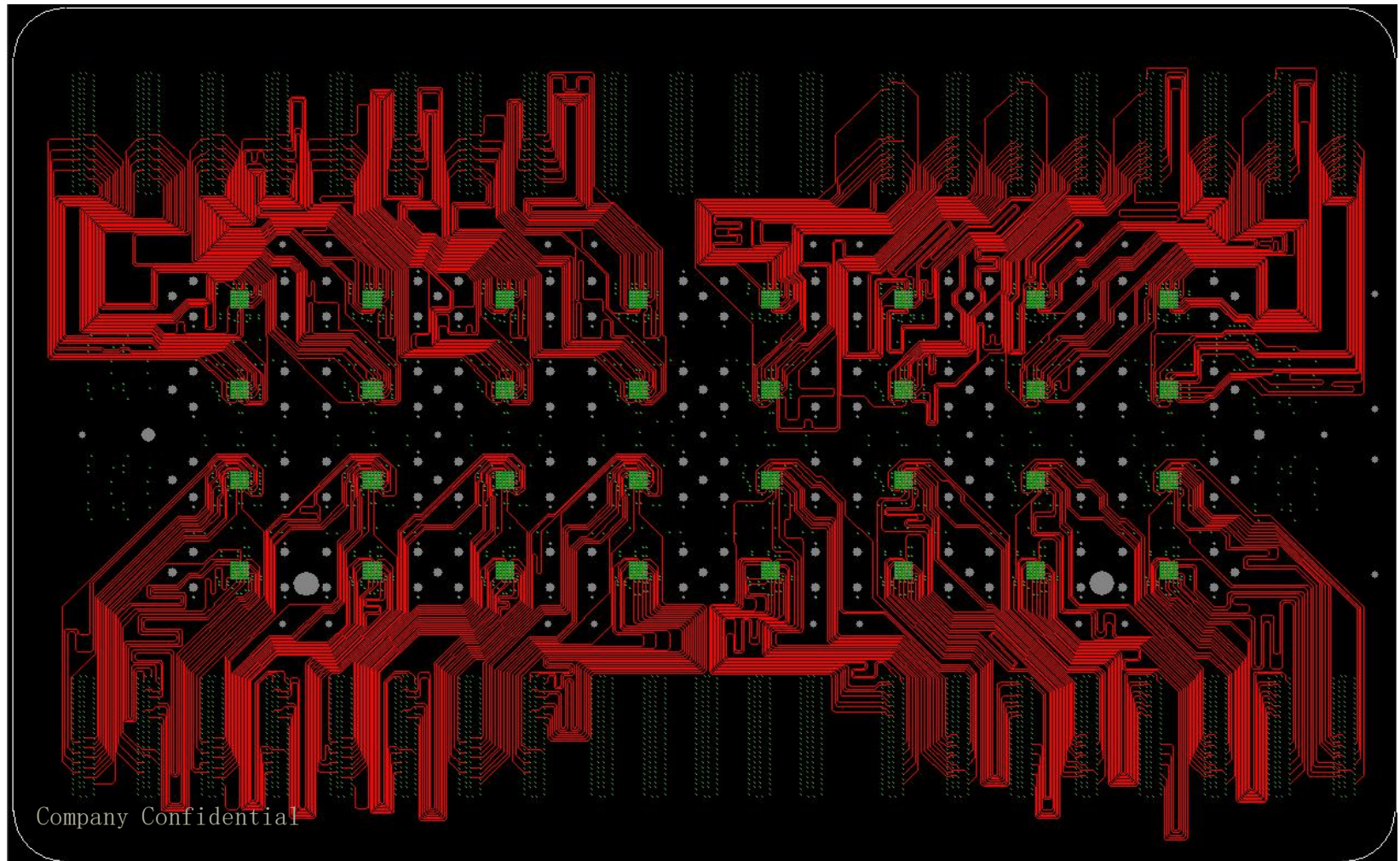


Component placement view



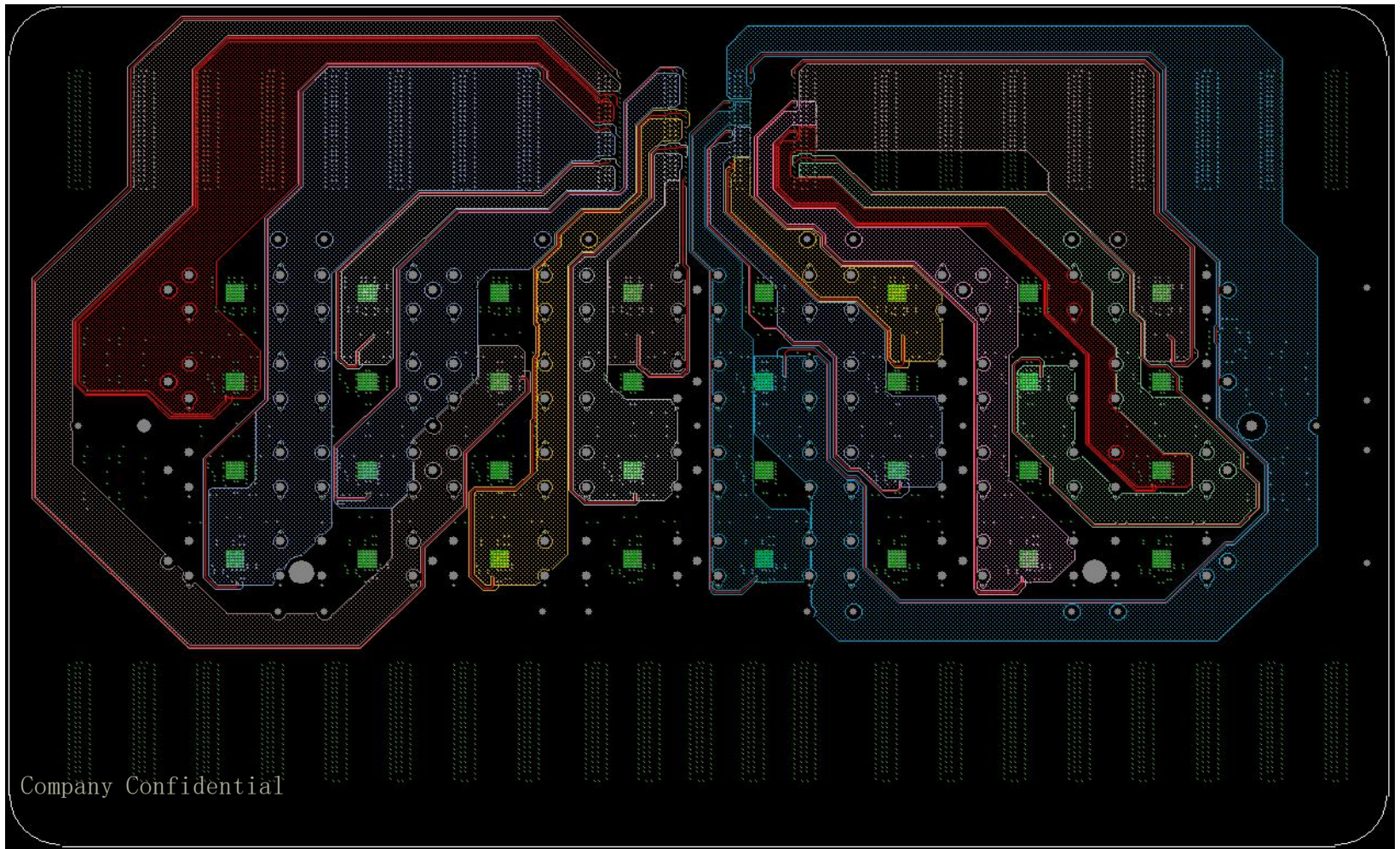


Inner layer routing image





Inner layer power image (senses routed parallel to shapes)





6.T6573 Loadboard

∞ **Net count** : 712 (including I/O & Power)

∞ **Layers** : 22 in total

∞ 6 I/O signal layers

∞ 1 Utility layer

∞ 5 Power layers

∞ **Component count** : 271

∞ **Highlights** :

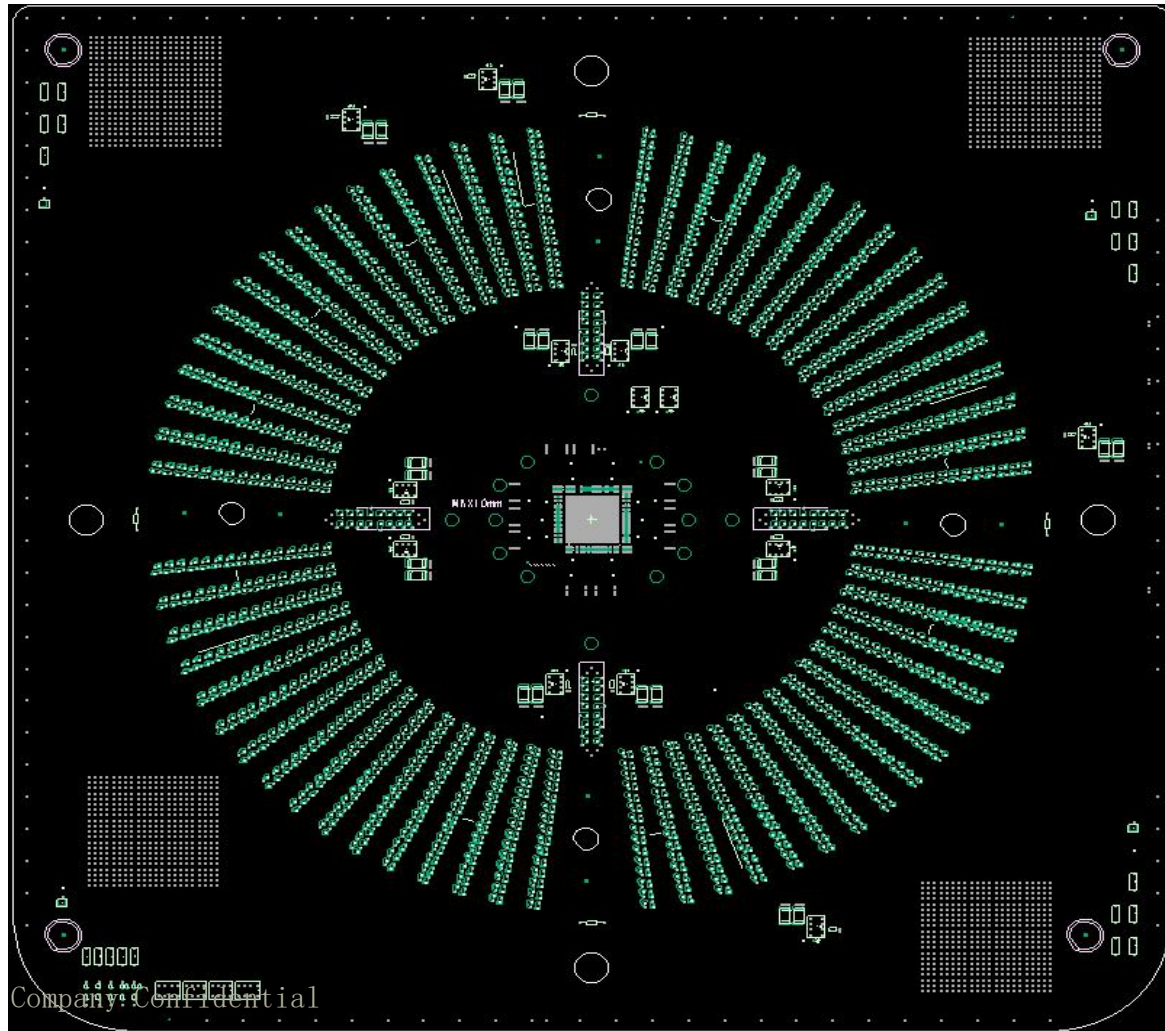
∞ Quick turnaround (1 day for schematic, 2 days for placement and routing)

∞ **Scope** : Schematic capture to Completed brd

∞ **Timeline** : 3 days (includes: Schematic capture to Completed brd
excludes : Customer review days)

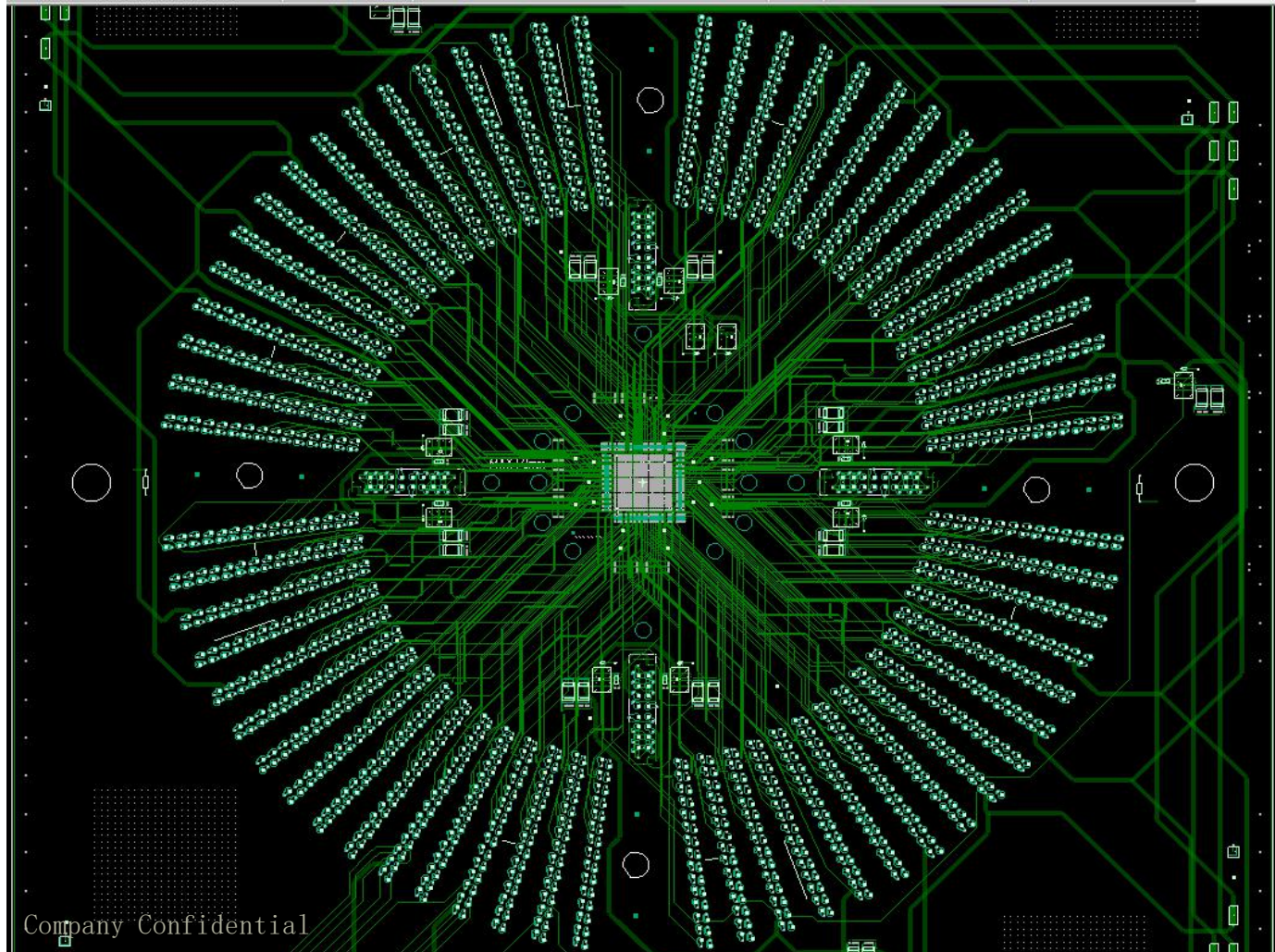


Placement image





Routing image





Probe Interface Boards

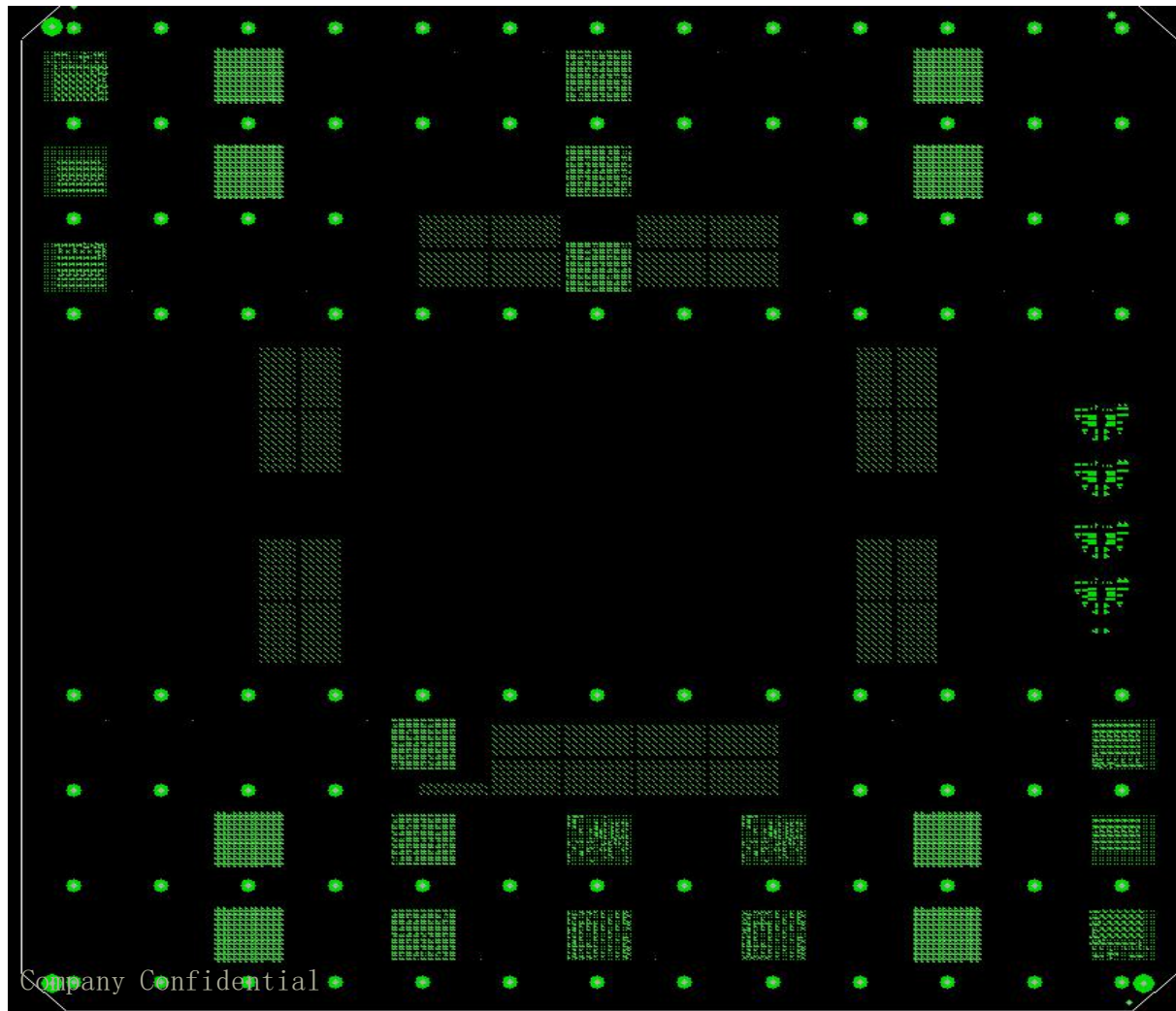


7. UltraFlex PIB

- ⌘ Net count : 1900 (including I/O & Power)
- ⌘ Layers : 28 in total
 - ⌘ 6 I/O signal layers
 - ⌘ 2 Utility layers
 - ⌘ 6 Power layers
- ⌘ Component count : 73
- ⌘ Highlights :
 - ⌘ Complete library developed in-house
 - ⌘ Validated Gerbers released for FAB
 - ⌘ Blind vias used at POGO interface area
- ⌘ Scope : Schematic capture to Gerbers
- ⌘ Timeline : 11 days (includes: Schematic capture to Gerbers
excludes : Customer review days)

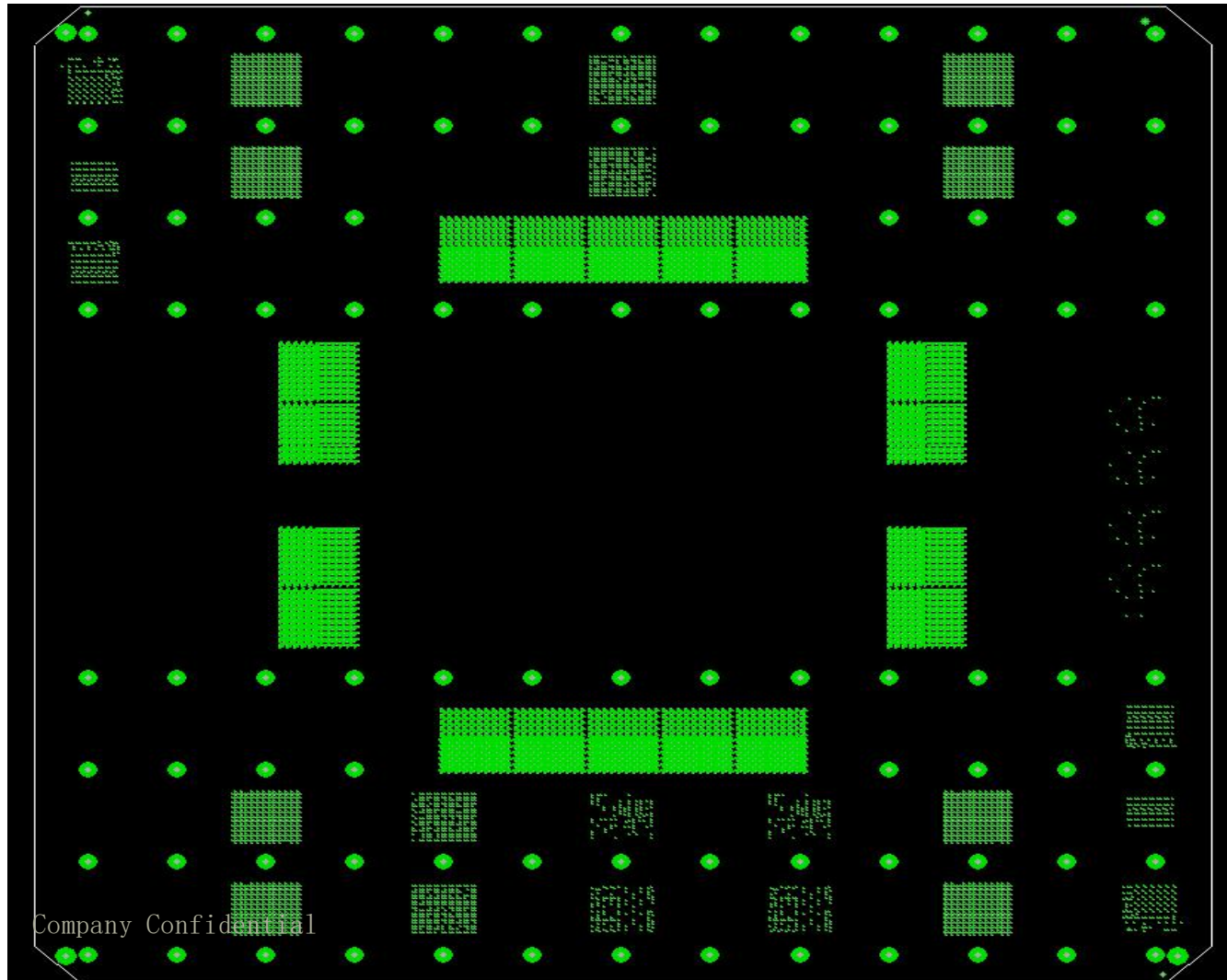


Top view



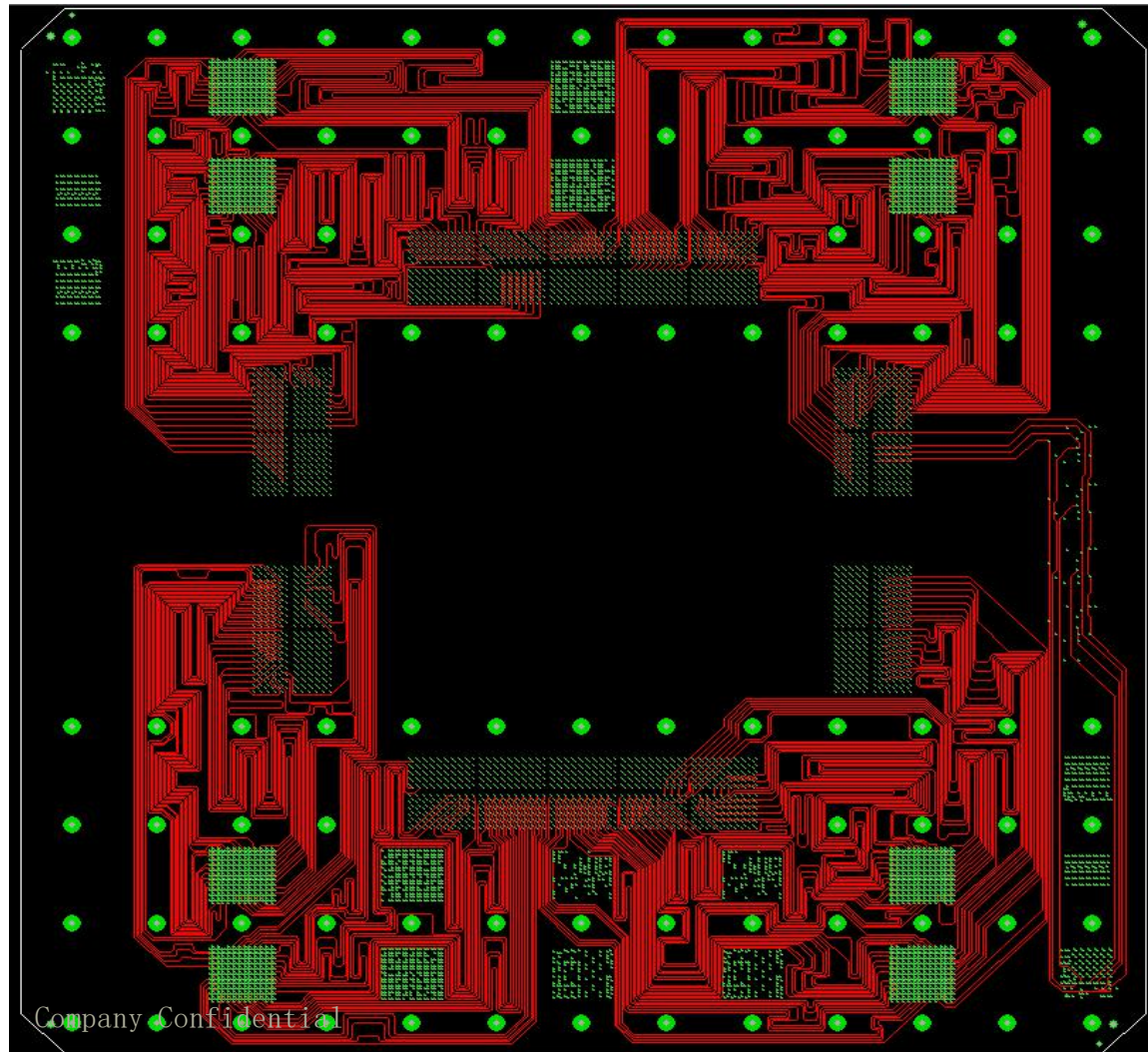


Bottom View





Signal layer



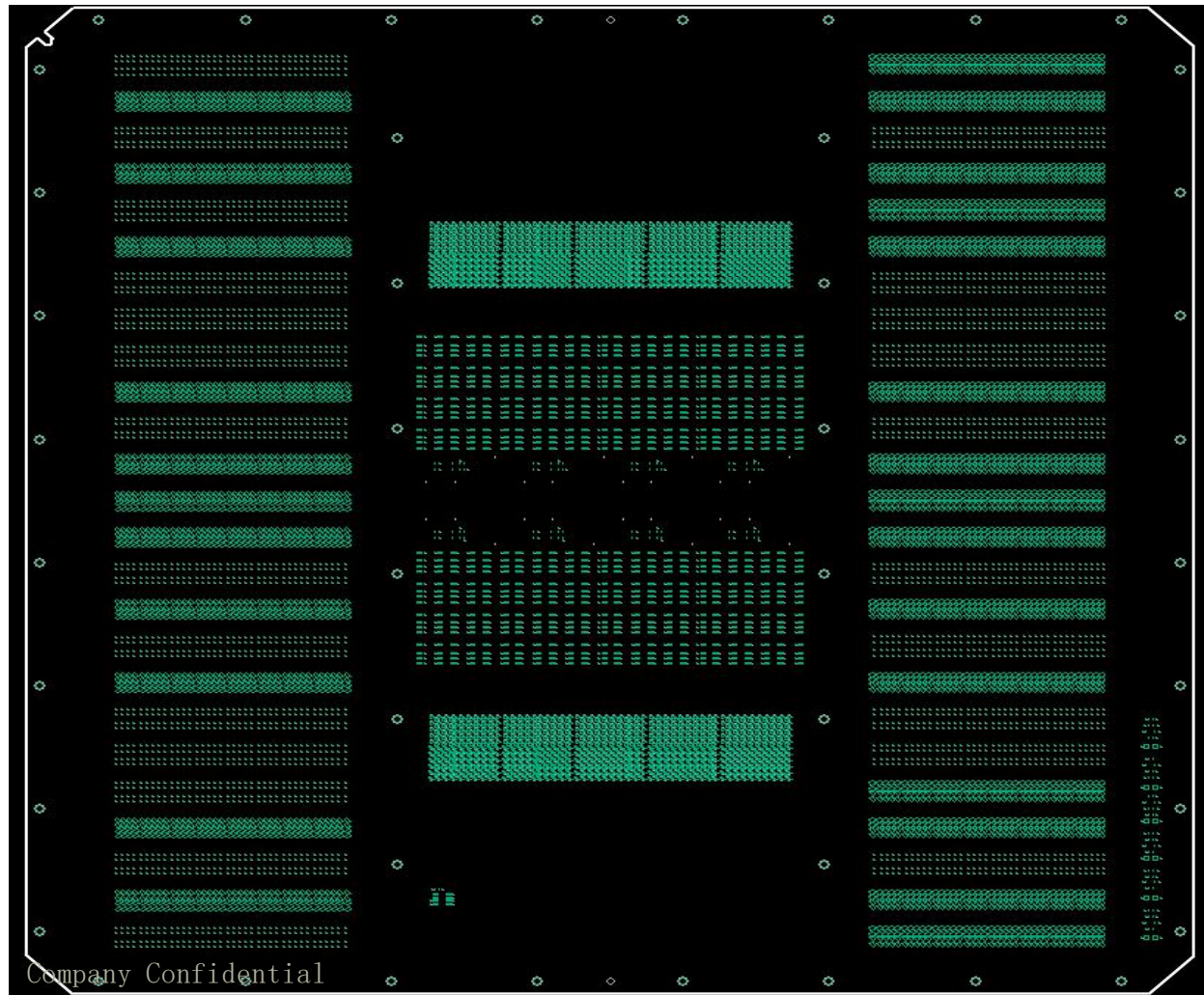


8. IntegraFLEX PIB

- ⌘ Net count : 774 (including I/O & Power)
- ⌘ Connections : closing to 2000
- ⌘ Layers : 24 in total
 - ⌘ 12 signal layers (including DCxx)
 - ⌘ 2 Power layers
- ⌘ Component count : 228
- ⌘ Highlights :
 - ⌘ Complete library developed in-house
 - ⌘ Multiple kelvin routing for DCxx resources
- ⌘ Scope : Schematic capture to Completed brd
- ⌘ Timeline : 7 days (Schematic capture to board completion)

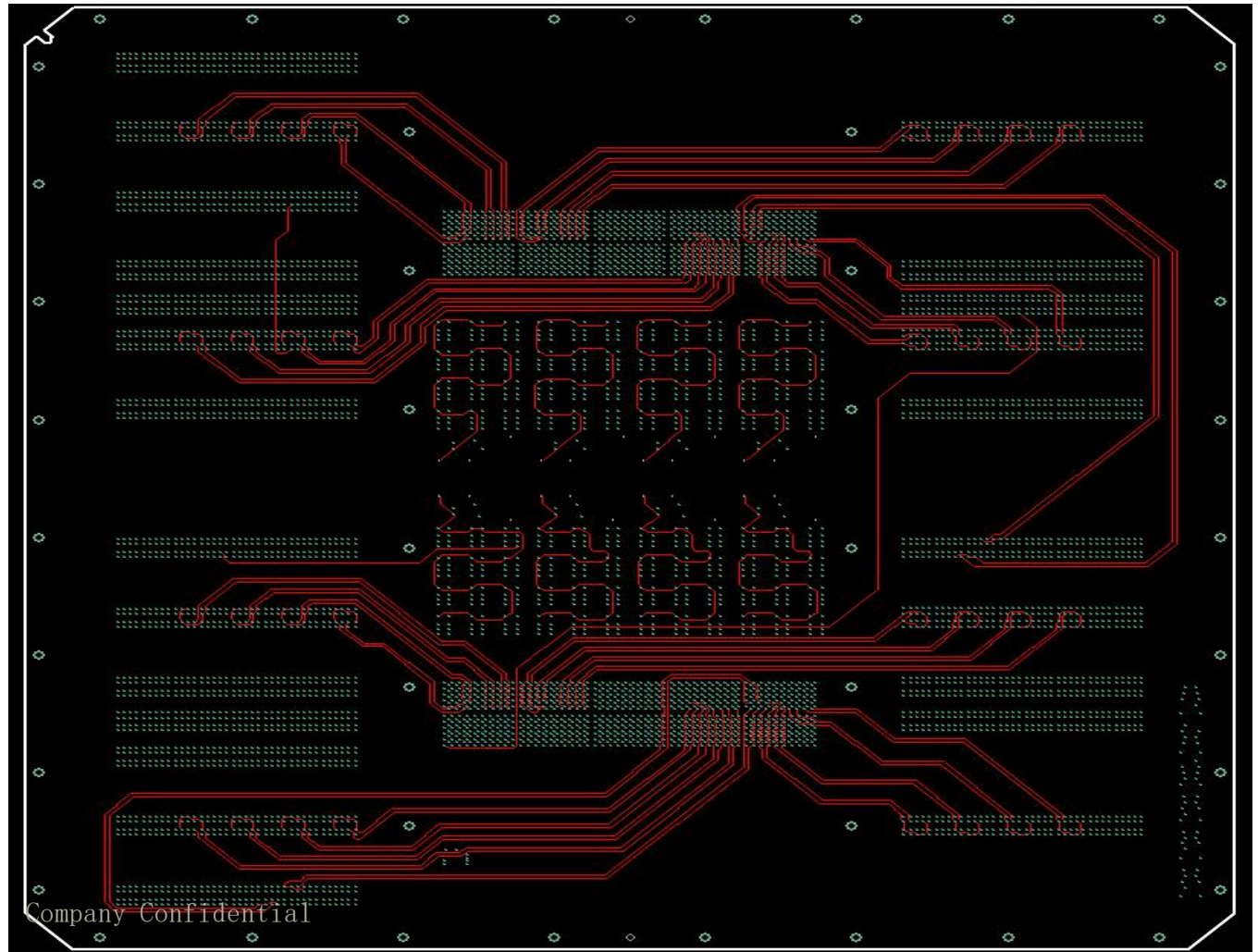


Component placement view





DCxx resource routing





Probe Cards

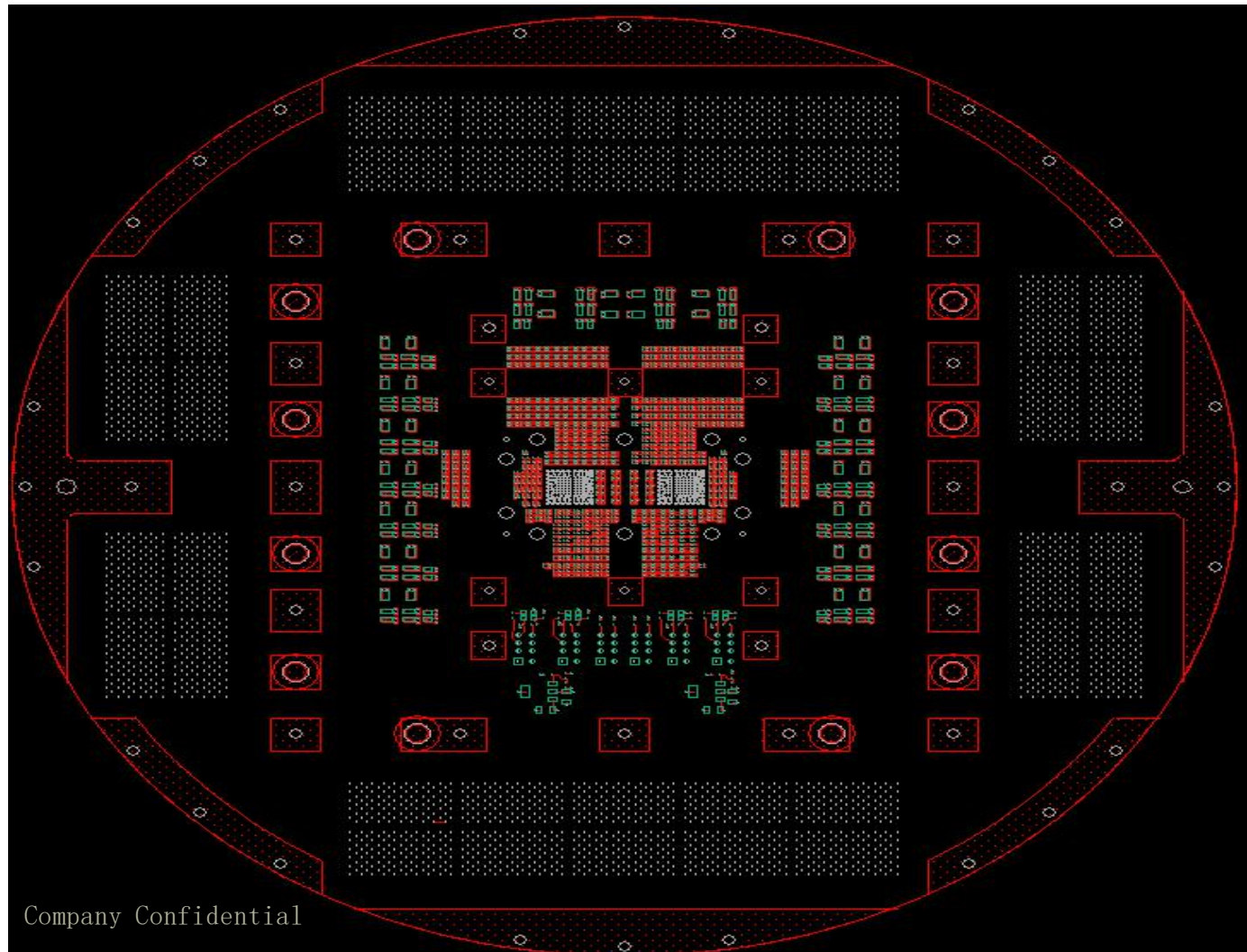


9. UltraFlex Probecard

- ⌘ Net count : 1200 (including I/O & Power)
- ⌘ Connections : closing to 2000
- ⌘ Layers : 28 in total
 - ⌘ 6 I/O signal layers
 - ⌘ 3 Sense/utility layers
 - ⌘ 6 Power layers
- ⌘ Component count : 594
- ⌘ Device pitch : 0.4 mm
- ⌘ Highlights :
 - ⌘ Fine pitch design
 - ⌘ Complete library developed in-house
 - ⌘ Validated Gerbers released to FAB
- ⌘ Scope : Schematic capture to Gerbers
- ⌘ Timeline : 7 days (Schematic capture to Gerbers)



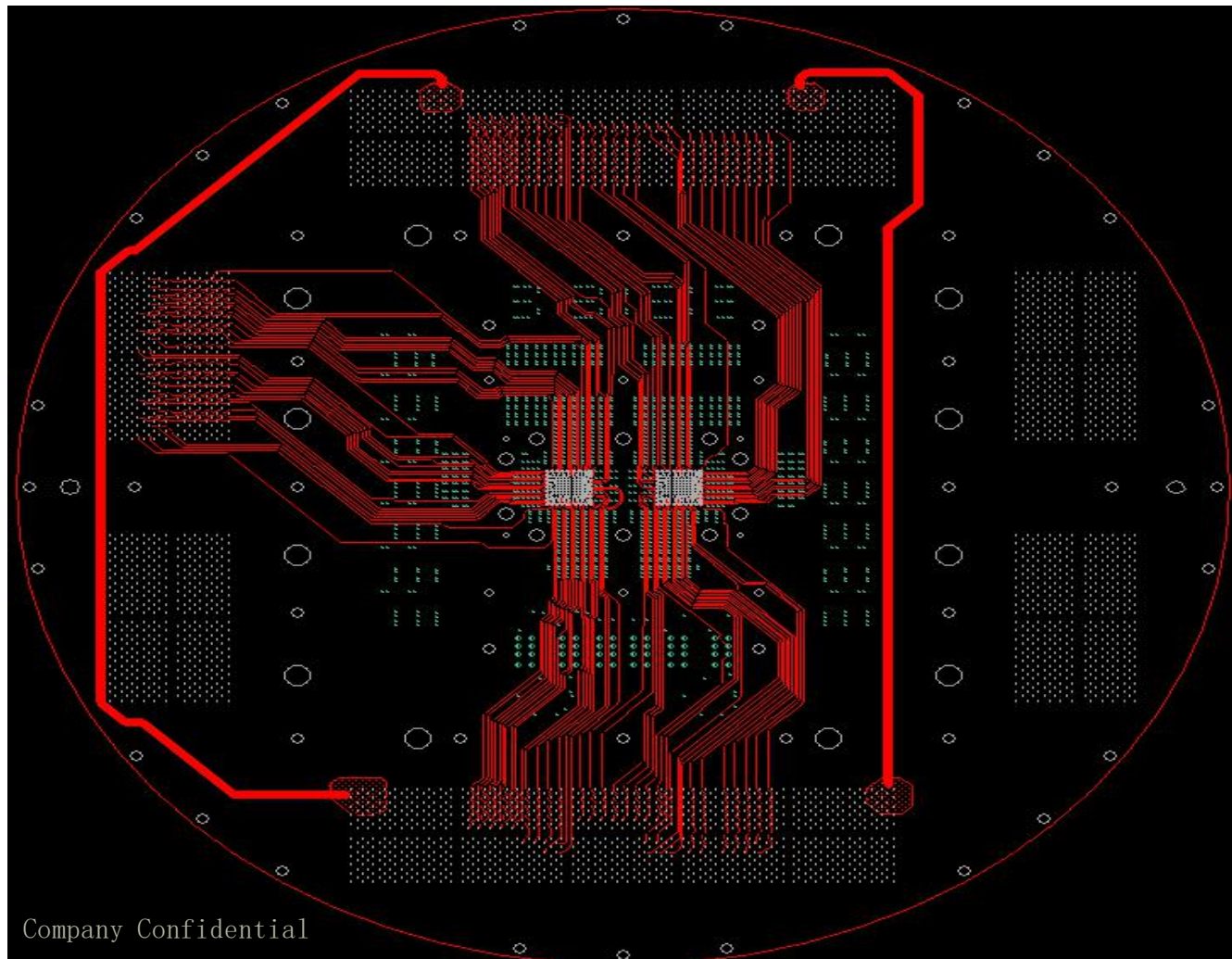
Component placement view



Company Confidential



Routing Layer



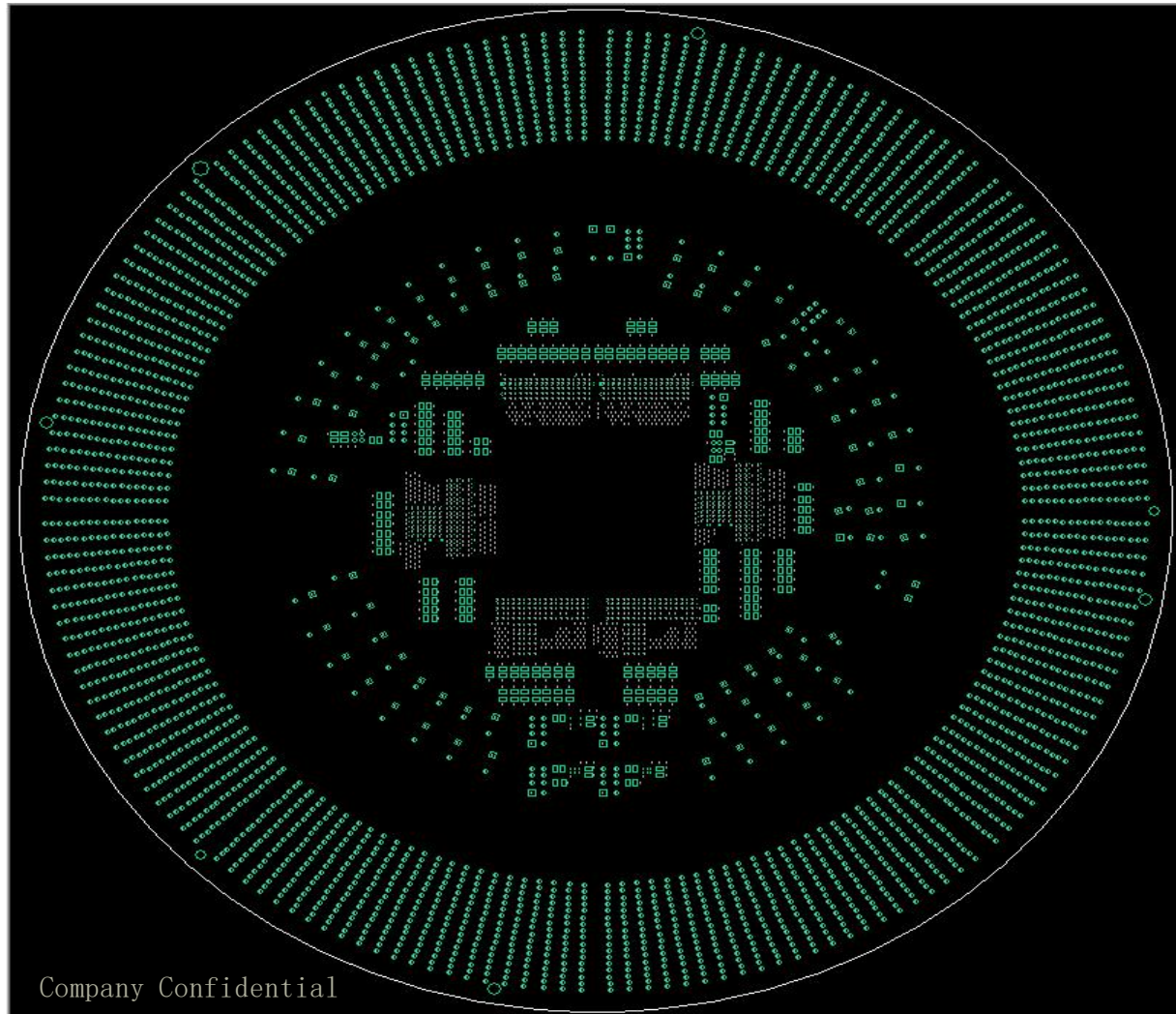


10. J750 Probecard

- ⌘ Net count : 1368 (including I/O & Power)
- ⌘ Connections : closing to 3500
- ⌘ Layers : 32 in total
 - ⌘ 8 I/O signal layers
 - ⌘ 6 DPS layers
 - ⌘ 2 sense/util layers
- ⌘ Component count : 242
- ⌘ Device pitch : 1.4 mm
- ⌘ Highlights :
 - ⌘ Complete library developed in-house
 - ⌘ Validated gerbers delivered to FAB
- ⌘ Scope : Schematic capture to Gerbers
- ⌘ Timeline : 7 days (includes: Schematic capture to Gerbers)

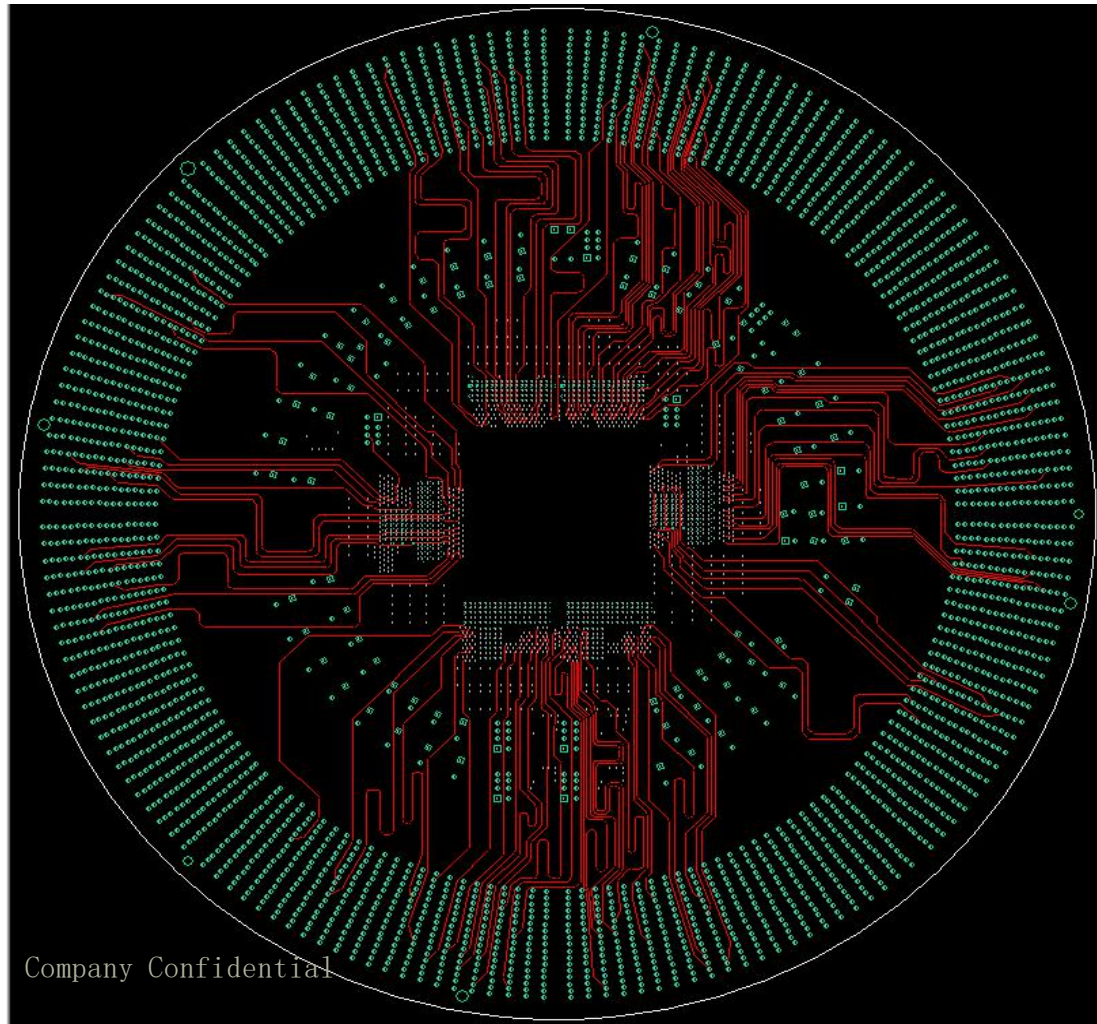


Component placement view





Inner layer routing image



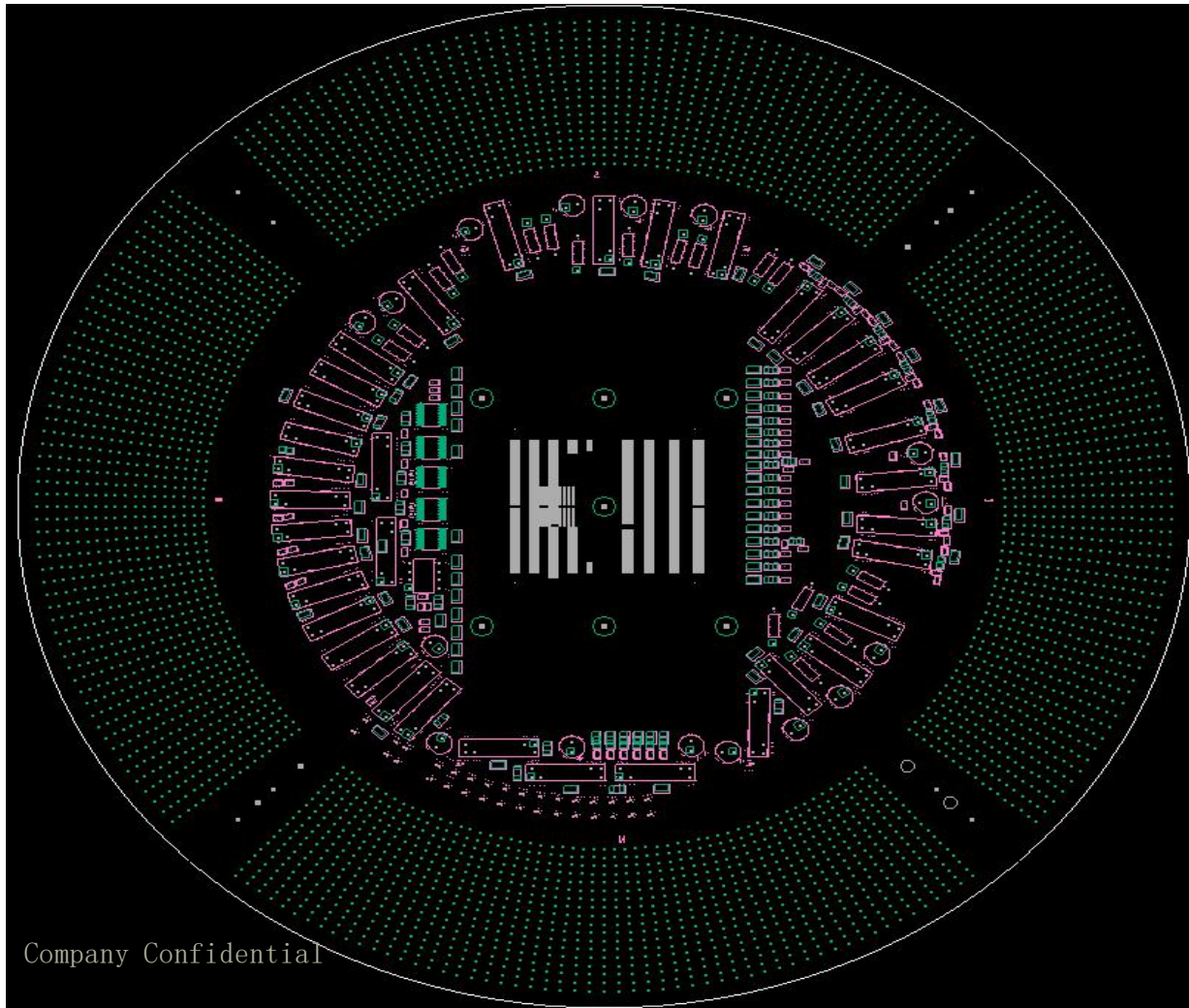


11.T6373 Probecard

- ⌘ Net count : 1850 (including I/O & Power)
- ⌘ Connections : closing to 2500
- ⌘ Layers : 46 in total
 - ⌘ 20 I/O signal layers
 - ⌘ 2 Sense/utility layers
 - ⌘ 6 Power layers
- ⌘ Component count : 359
- ⌘ Device pitch : 0.65 mm
- ⌘ Highlights :
 - ⌘ Complete library developed in-house
 - ⌘ Validated Gerbers released to FAB
- ⌘ Scope : Schematic capture to Gerbers
- ⌘ Timeline : 8 days (Schematic capture to Gerbers)



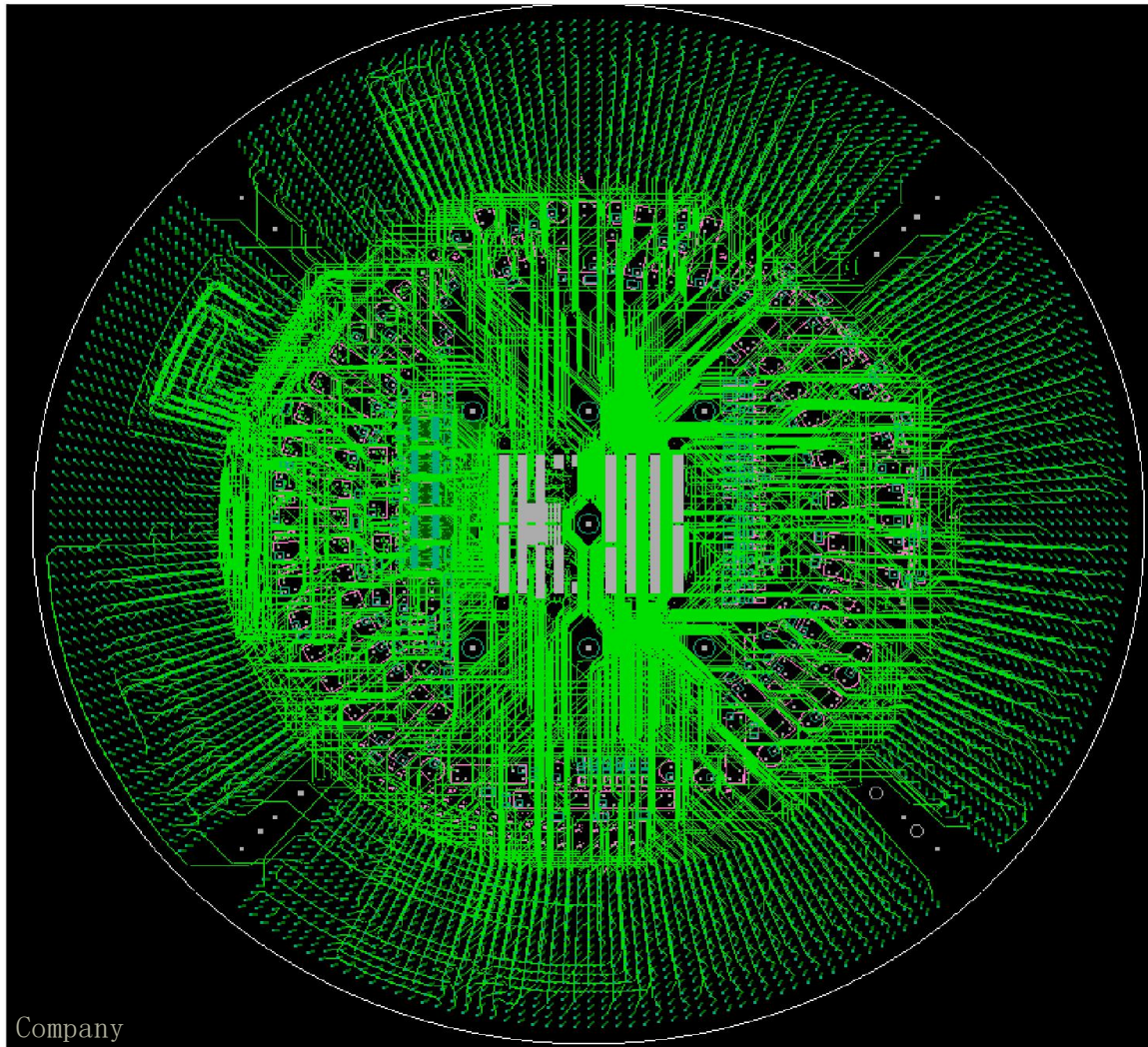
Component placement view



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Routing Layers



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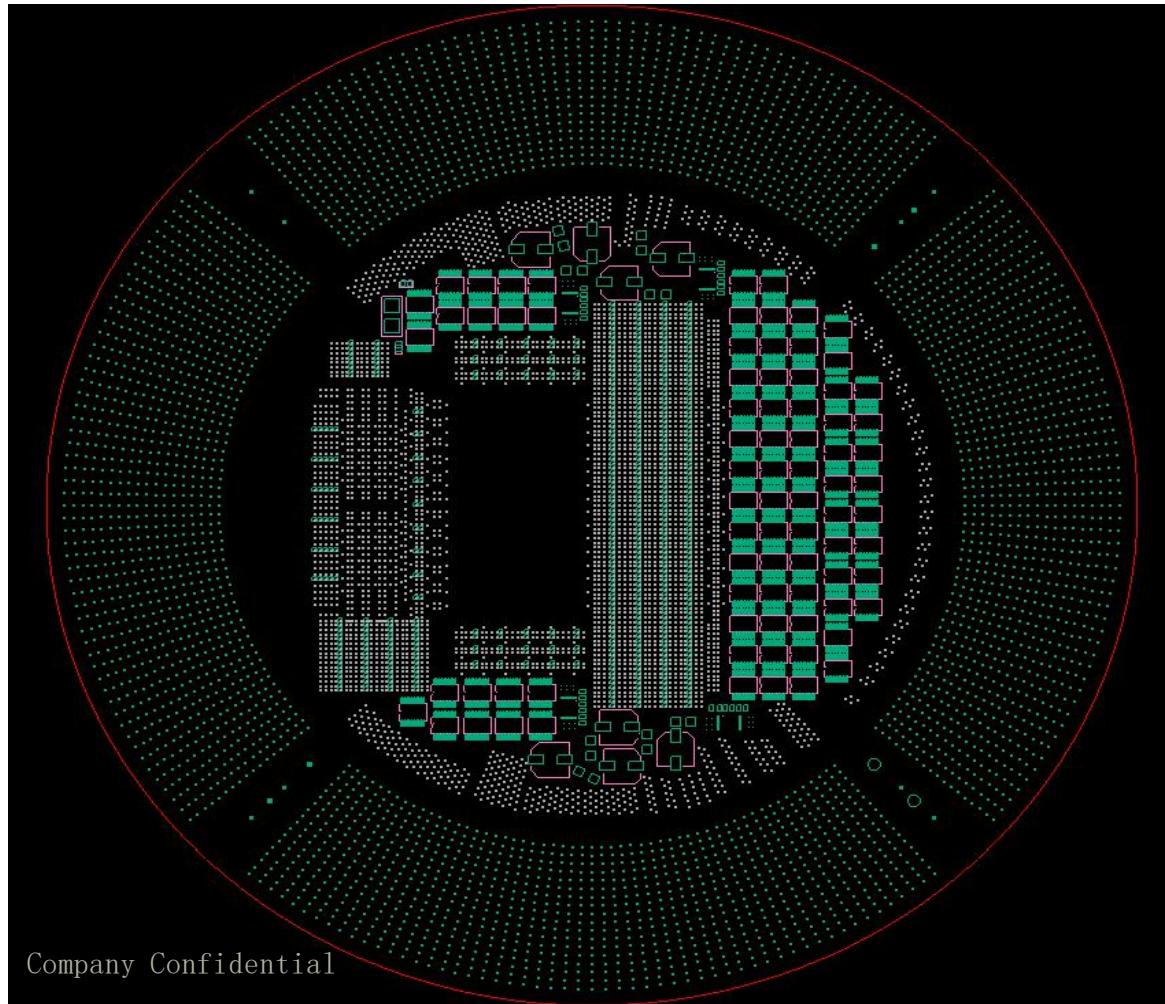


12.T6372 ProbeCard

- ⌘ Net count : 3200 (including I/O & Power)
- ⌘ Connections : closing to 4800
- ⌘ Layers : 44 in total
 - ⌘ 24 I/O signal layers
 - ⌘ 4 Power layers
- ⌘ Component count : 314
- ⌘ Device pitch / Pin count : 1.5 mm / 3200pins
- ⌘ Highlights :
 - ⌘ Complete library developed in-house
 - ⌘ Validated Gerbers released to FAB
- ⌘ Scope : Schematic capture to Gerbers
- ⌘ Timeline : 10 days (Schematic capture to Gerbers)



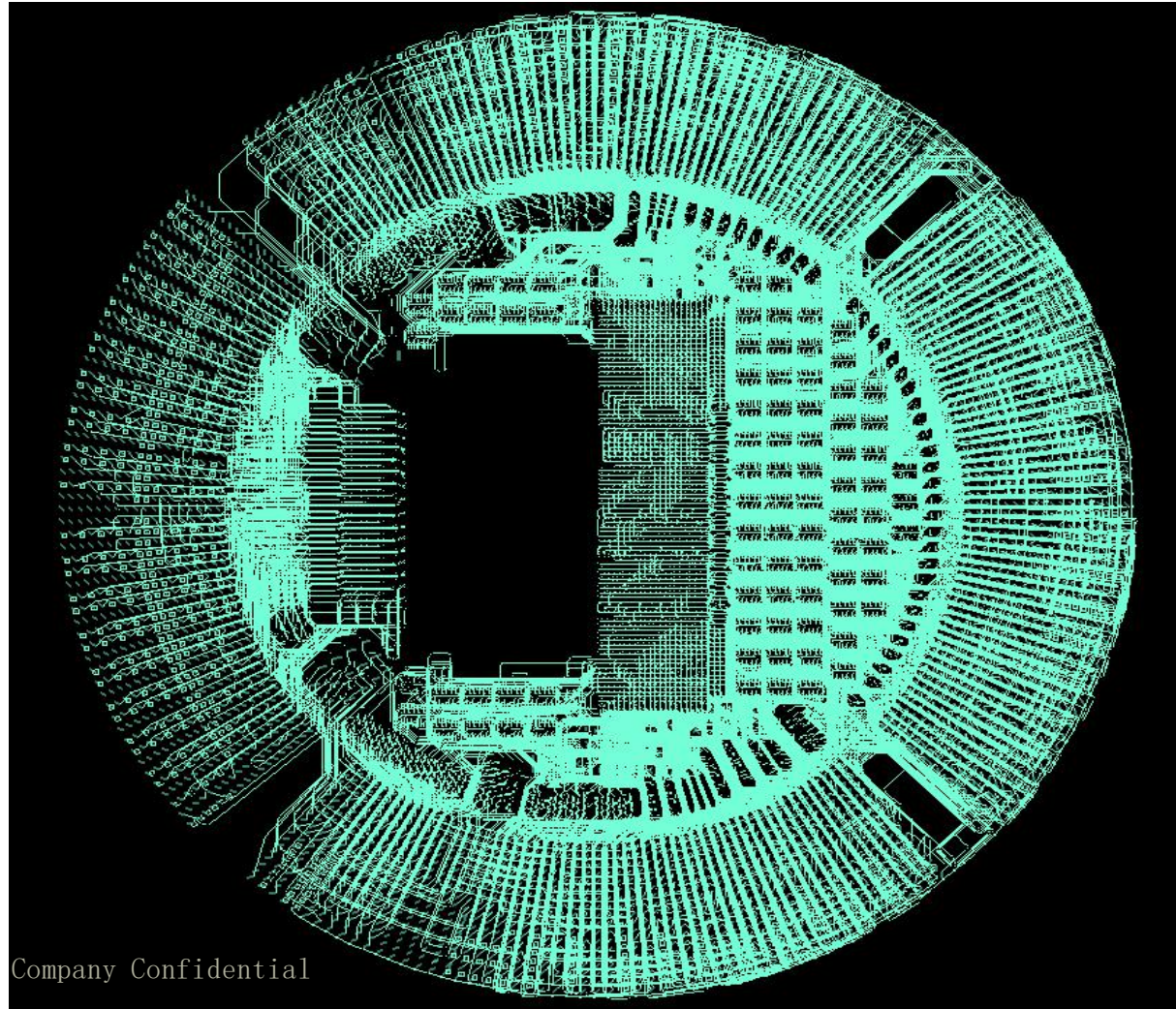
Component placement view



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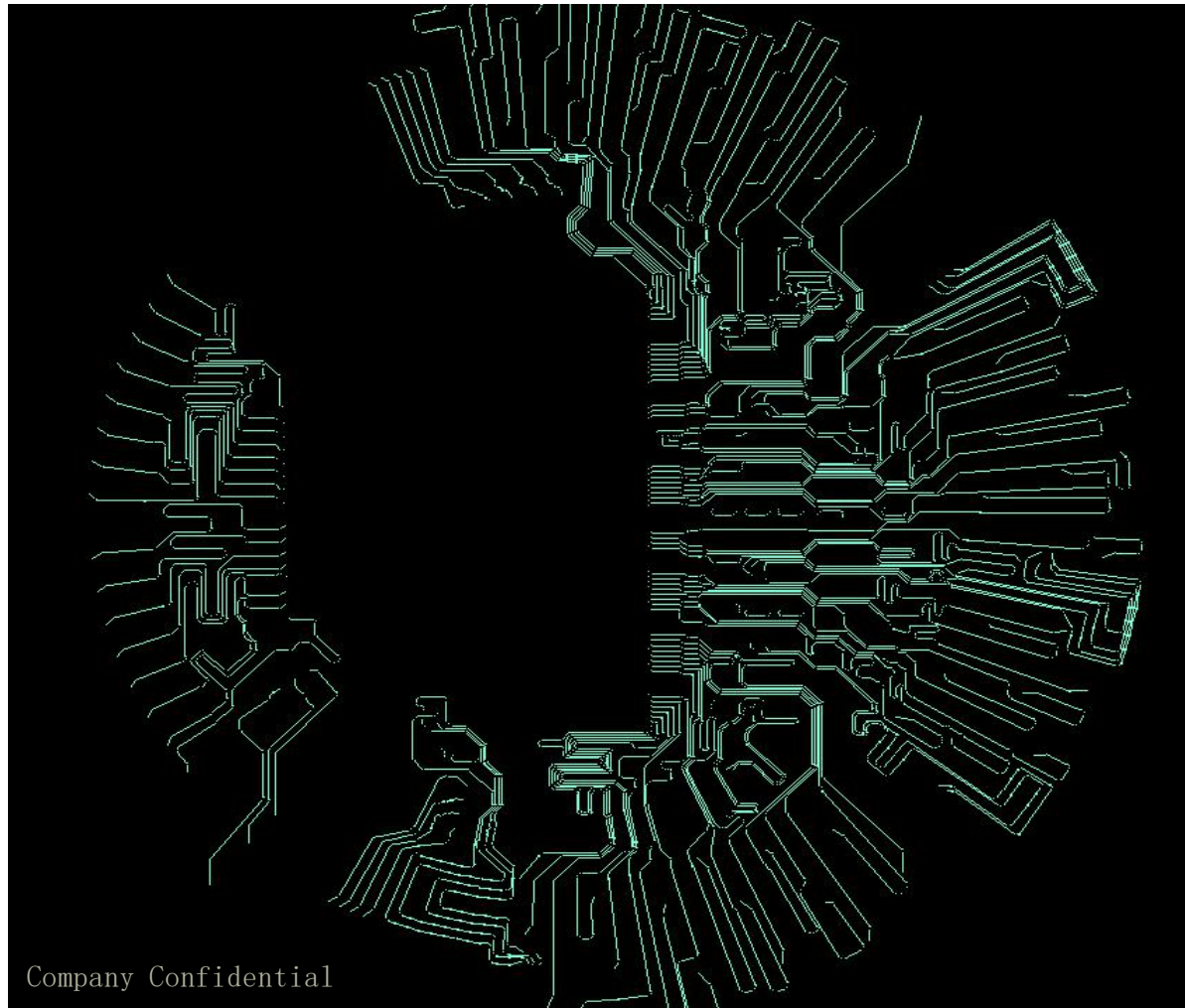
Routing Layers



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Single layer traces for closer look





NOTE

- ⌘ The timeline mentioned here is based on Standard Run, hot run can be done for Layout part on demand (which will be much faster to complete your routing requirements)
- ⌘ Please feel free to ask for any particular information in detail, for example detailed report of any sample shown here or additional samples on the platforms which have not been discussed here



Quick summaries

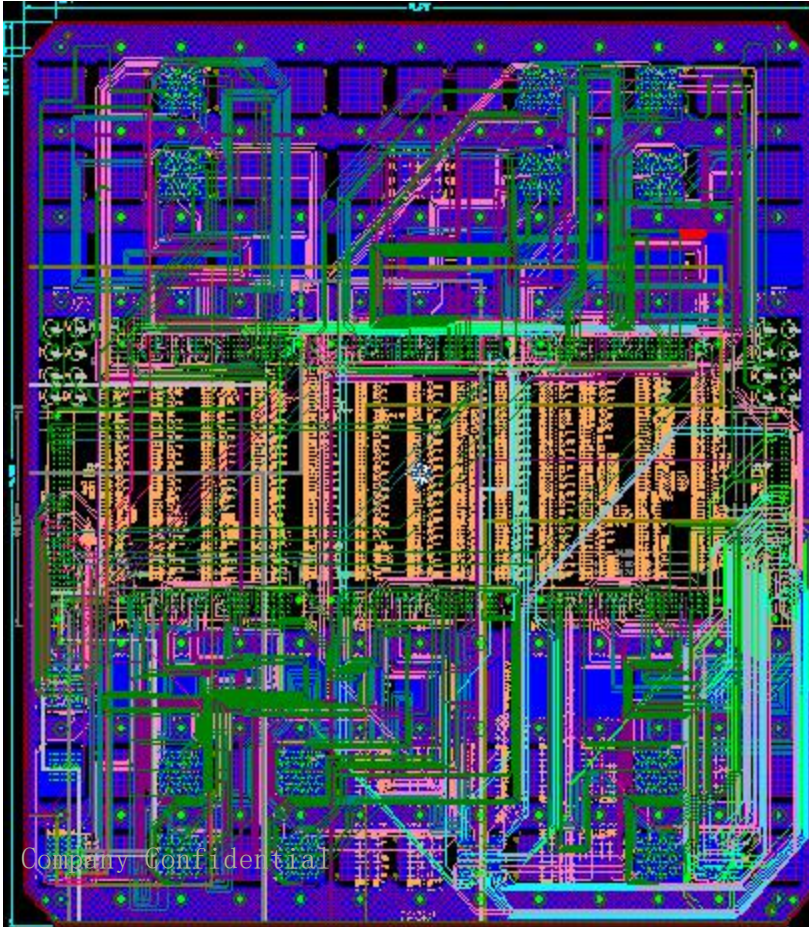


TEST BOARD EXCERPTS

LOAD BOARDS



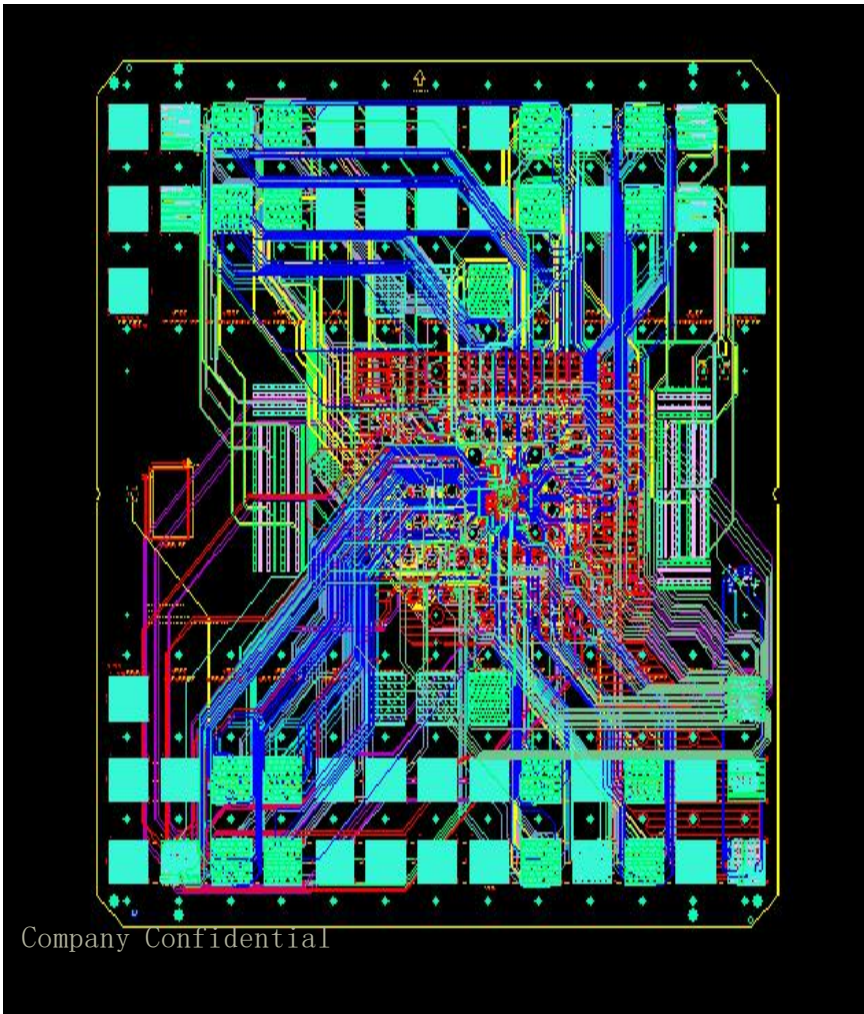
TERADYNE ULTRAFLEX – LOAD BOARD



- MOTHER BOARD
- All connections are Dedicated routing
- 2.54 mm pitch DUT socket
- VHFAC, HSD, DC30, POOL instruments are used
- 50 Ohm controlled impedance
- Delay matching for HSD signals
- Pin mapping mentioned in the silk
- 24 layers
- Material:FR4
- 148 mils BoardThickness



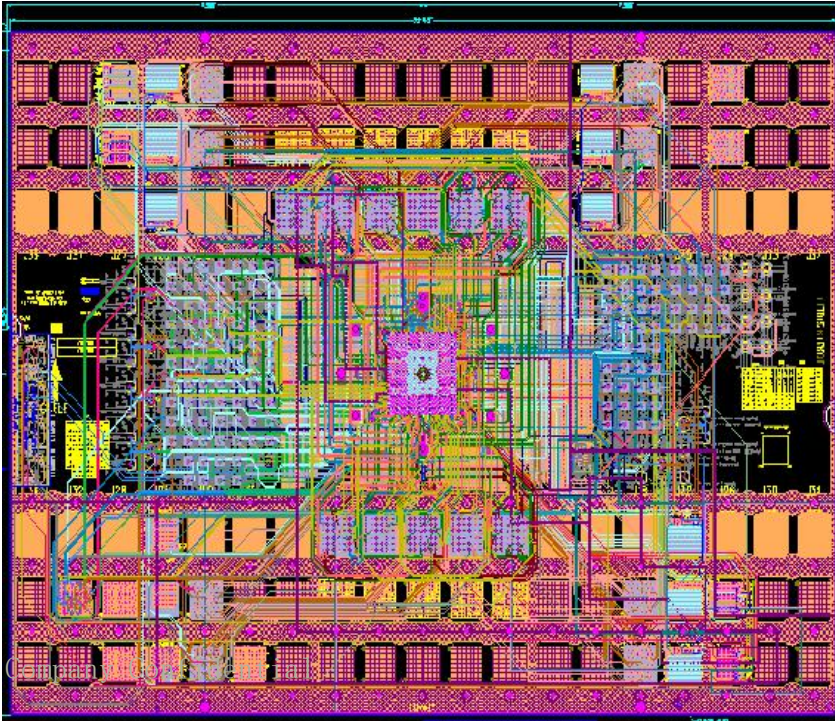
TERADYNE ULTRAFLEX – LOAD BOARD



- Single Site, 812 pin BGA
- 0.8mm pitch, Mixed Signal Device
- SB6G, ULTRAPIN800, BBAC, DC30 Instruments were used
- Separate Force & return planes for HEXVS Powers with 2 Oz copper thickness
- Back Drilling for High speed signal vias
- 28 layers
- Material: ROGERS4350 & Nelco4000-13 SI
- 4.75mm Board Thickness



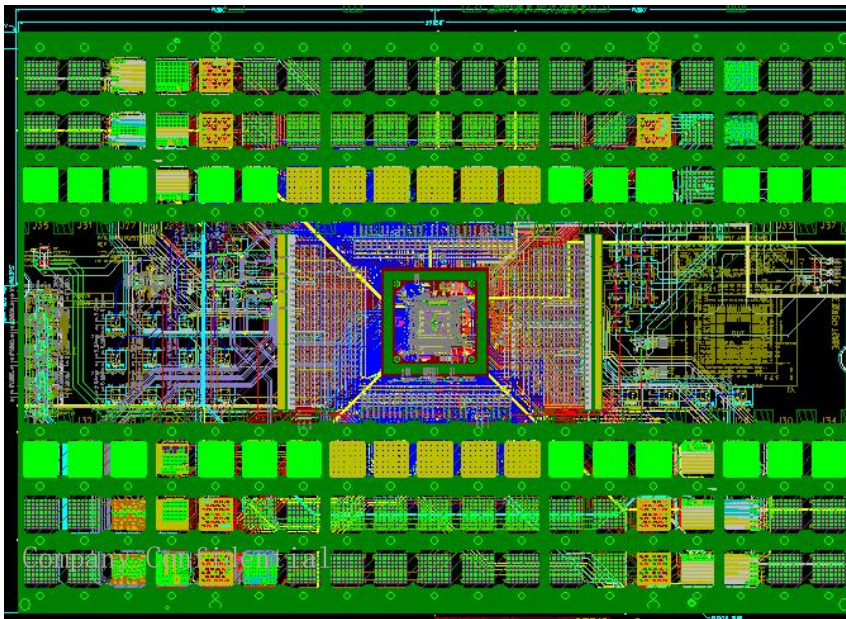
TERADYNE ULTRAFLEX – LOAD BOARD



- Single Site
- 1 mm pitch, 2304 pins BGA
- Loop back signals
- 50 & 100 Ohm controlled impedance
- 42 layers, RF connector, 2000 COMPONENTS used
- Material: ROGERS4350 & Nelco4000-13 SI
- 4.75mm BoardThickness



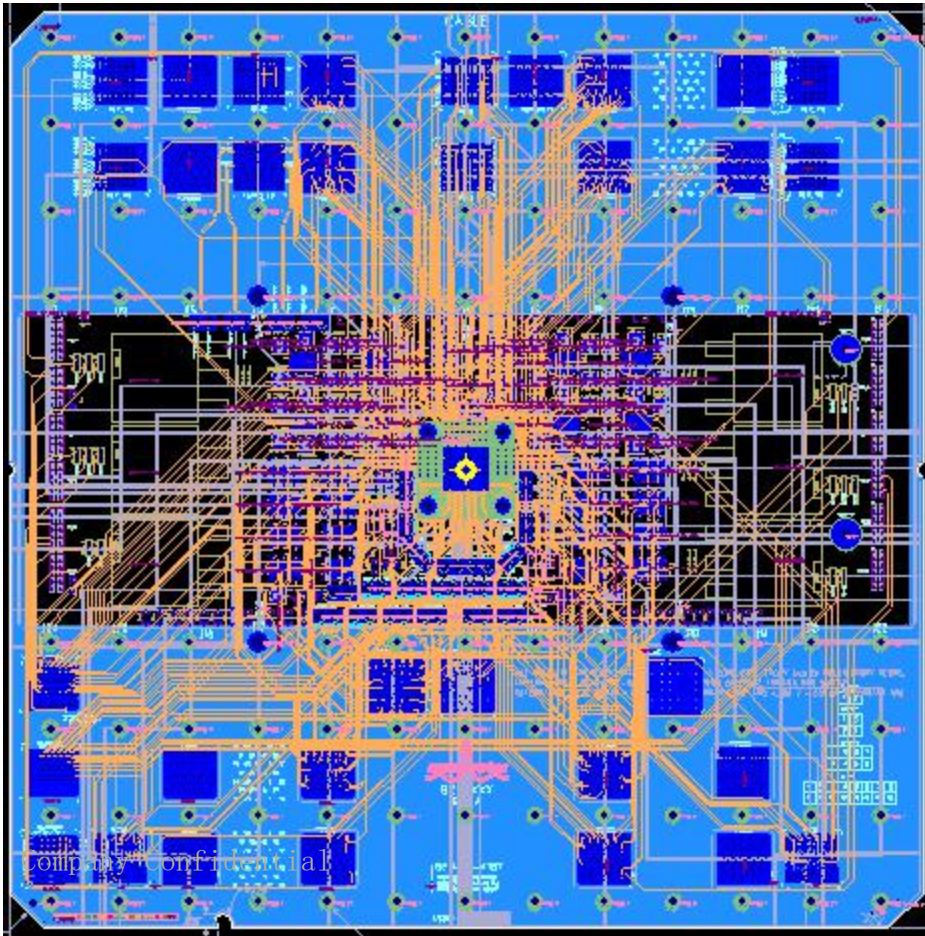
TERADYNE ULTRAFLEX – LOAD BOARD



- Single Site, 1348 pin BGA
- 1.0mm pitch, Mixed SignalDevice
- 780 signals
- 50 & 100 Ohm Controlled Impedance
- Delay matching for HSD signals
- 42 layers
- Material: Nelco4000-13SI, Rogers 4350 used for first 15 layers right from TOP
- 6.6 MM BoardThickness



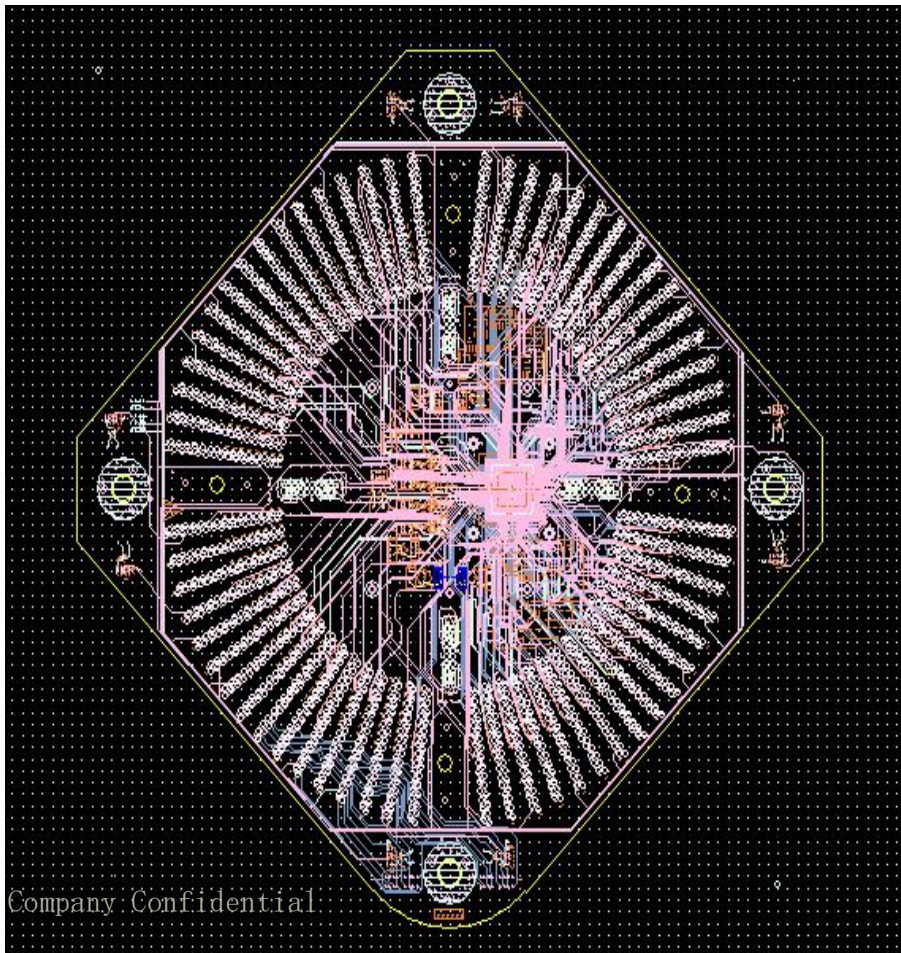
TERADYNE ULTRAFLEX – LOAD BOARD



- Single Site, BCM8747-BGA-21x21 BGA
- 1mm pitch, Digital Device
- RELAY_ARJ20A12_12VDC
- 8GHZ_2FORMC Relays used
- RF connector used
- 50 Ohm Controlled Impedance
- Delay matching
- 38 layers
- Material: Rogers 4003C outer dielectrics, inner is FR4.
- 4.75mm Board Thickness



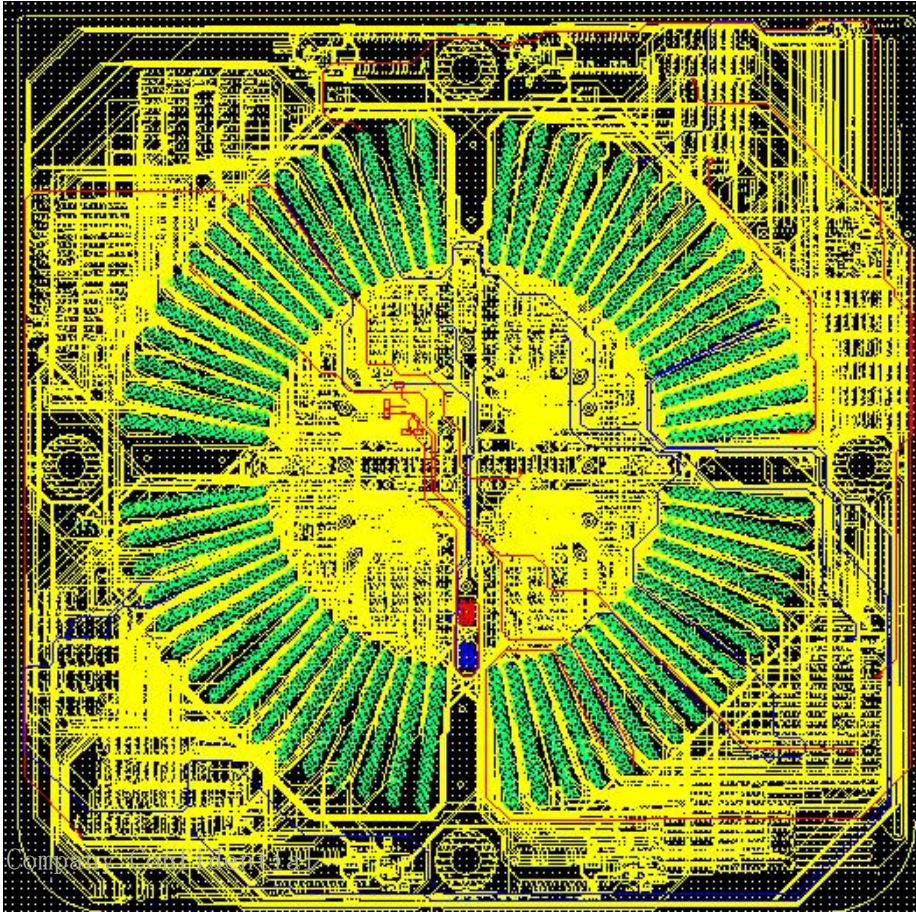
ADVANTEST T6682 – LOAD BOARD



- SINGLE SITE
- BGA -985 PINS, 1MM PITCH
- 500 NETS
- 50 ohm controlled
- impedance 26layers
- Material:Nelco-4000-13-SI
- 4.8mm BoardThickness



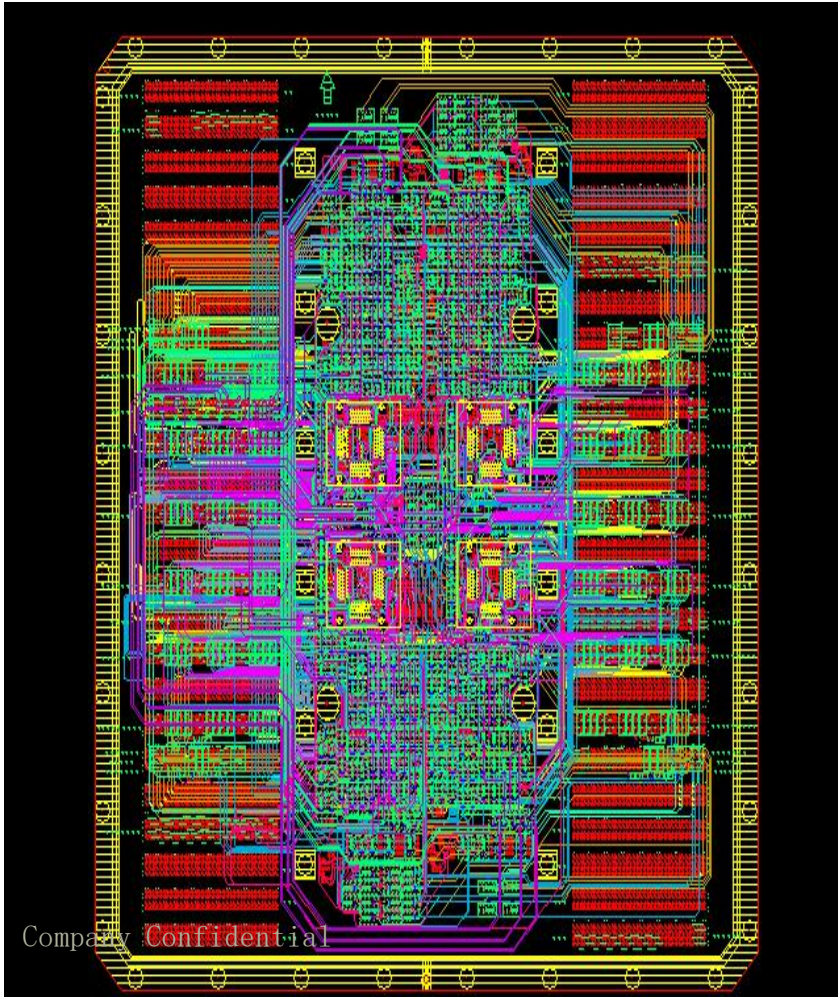
ADVANTEST T6573 – LOAD BOARD



- QUAD SITE
- BGA 164 PINS, 0.5MM PITCH
- 50 ohm controlled impedance
- 1500 COMPONENTS
- 1800 SIGNALS
- 30 layers
- Material: Nelco-4000-7-SI
- 4.8mm Board Thickness



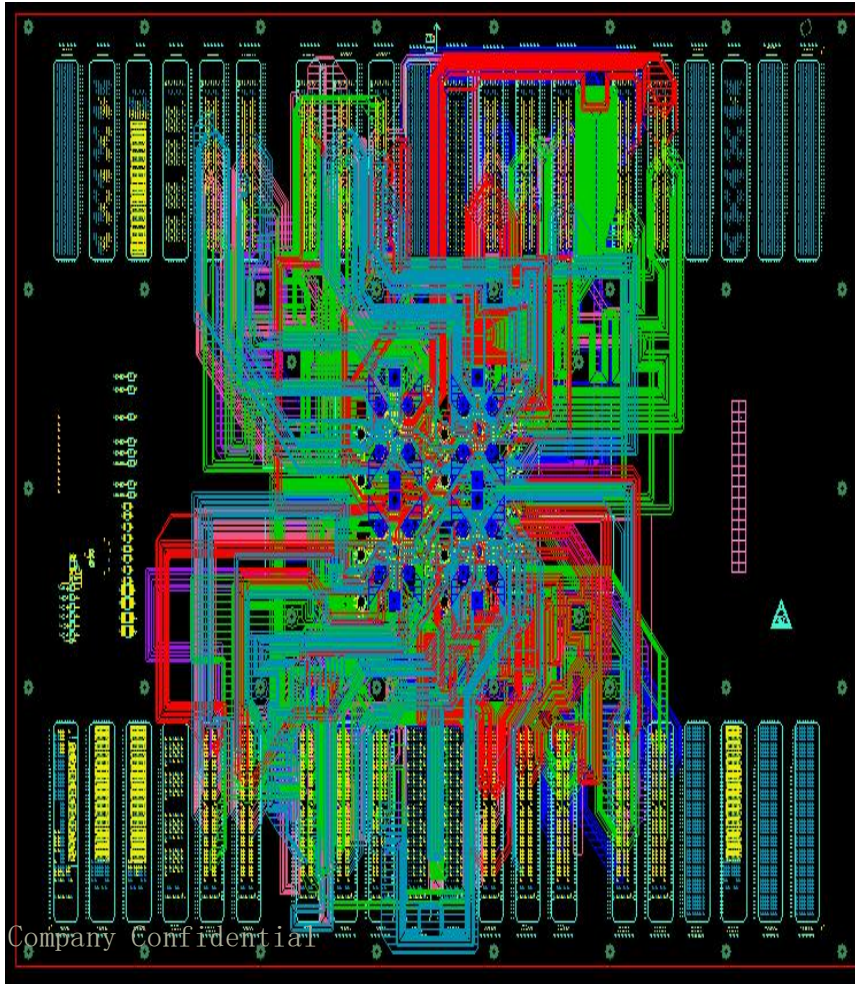
TERADYNE FLEX – LOAD BOARD



- Quad site
- 0.5mm pitch, Mixed signal Device
- VHFAC, HSD, DC30, POOL instruments are used
- 50 & 100 Ohm controlled impedance
- Delay matching for all signals
- Shape shielding for all critical nets
- 334 relays out of 1056 components
- 30 layers
- Material: Nelco4000-13 SI & FR4
- 5.08mm Board Thickness



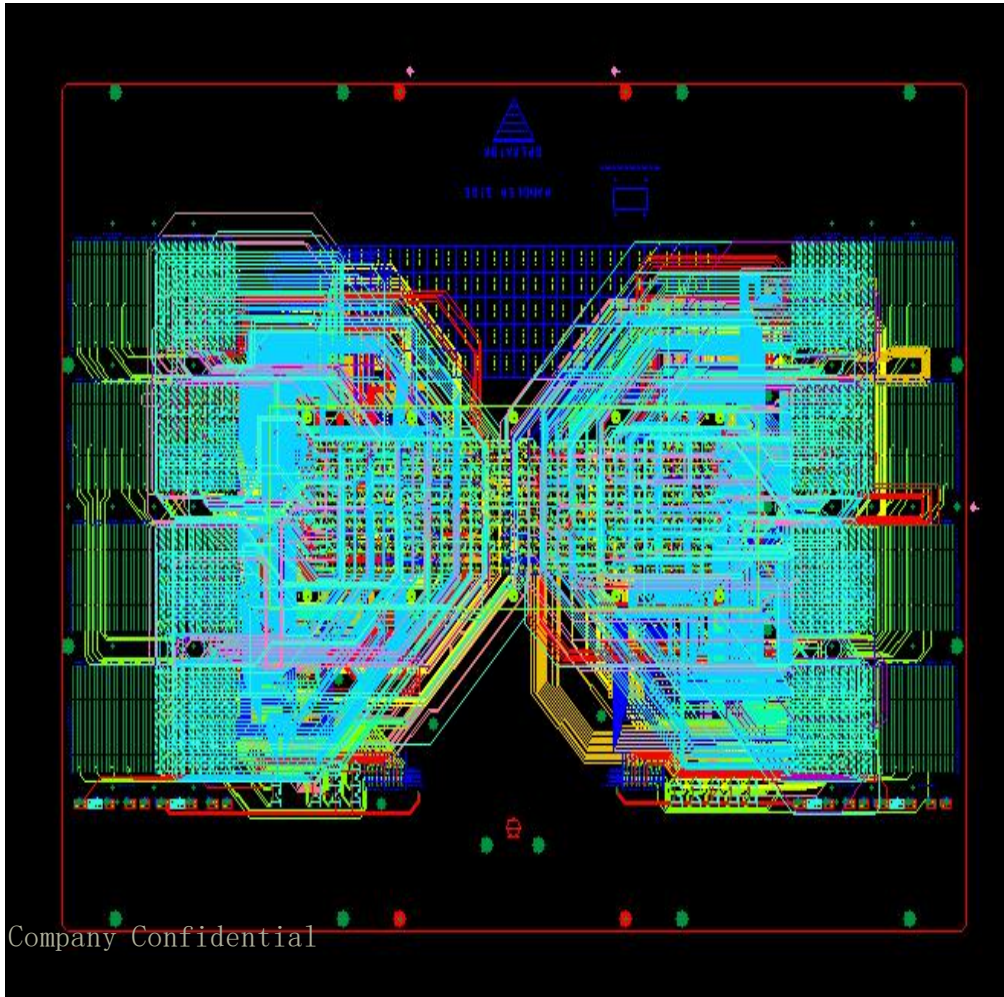
CREDENCE SAPPHIRE – LOAD BOARD



- Quad Site, 581 pin BGA
- 0.4mm pitch, Mixed Signal Device
- 1240 signals
- 20-D2064 instruments were used
- 50 & 100 Ohm Controlled Impedance
- Delay matching for all signals
- Shape shielding for all critical nets
- Blind vias were used
- 32 layers
- Material: Nelco4000-13 SI
- 4.75mm Board Thickness



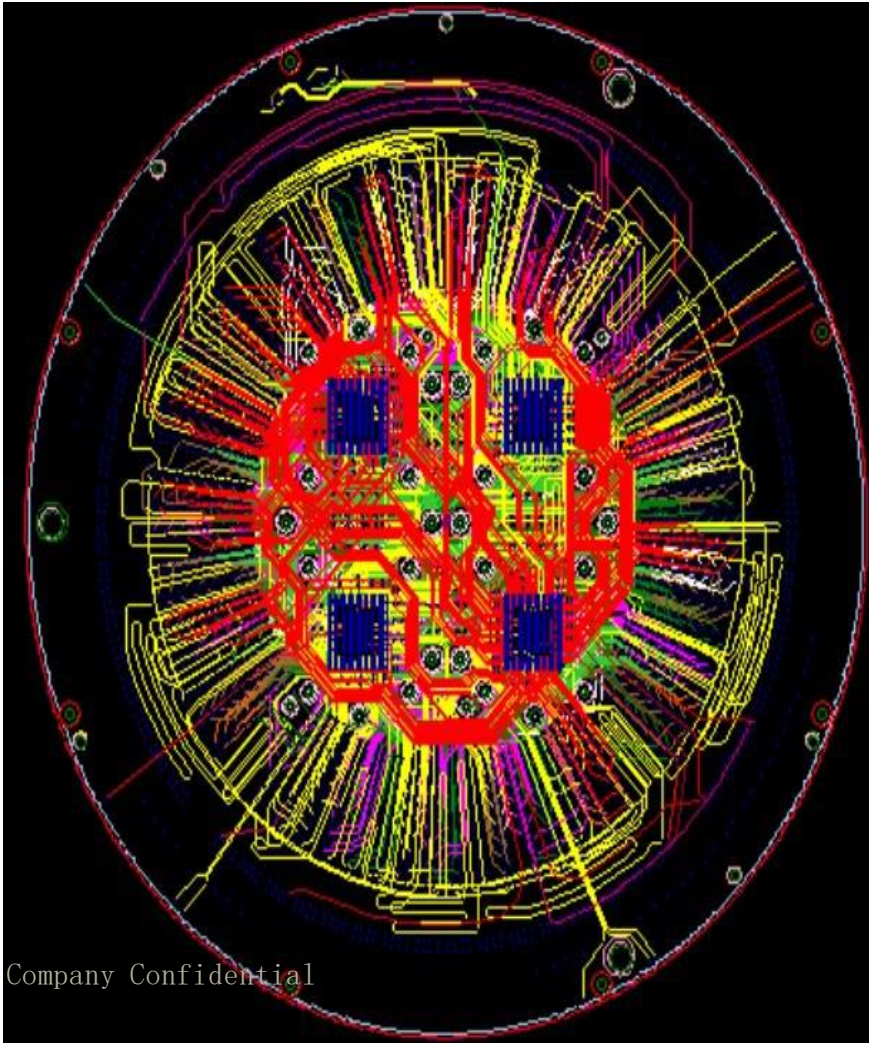
NEXTEST MAGNUM – LOAD BOARD



- 140 Sites
- 8 Pins/Site
- 840 signals
- 50 ohm controlled impedance
- Delay matching for all signals
- 140 powers
- 26 layers
- Material:Fr4
- 6.35mm Board Thickness



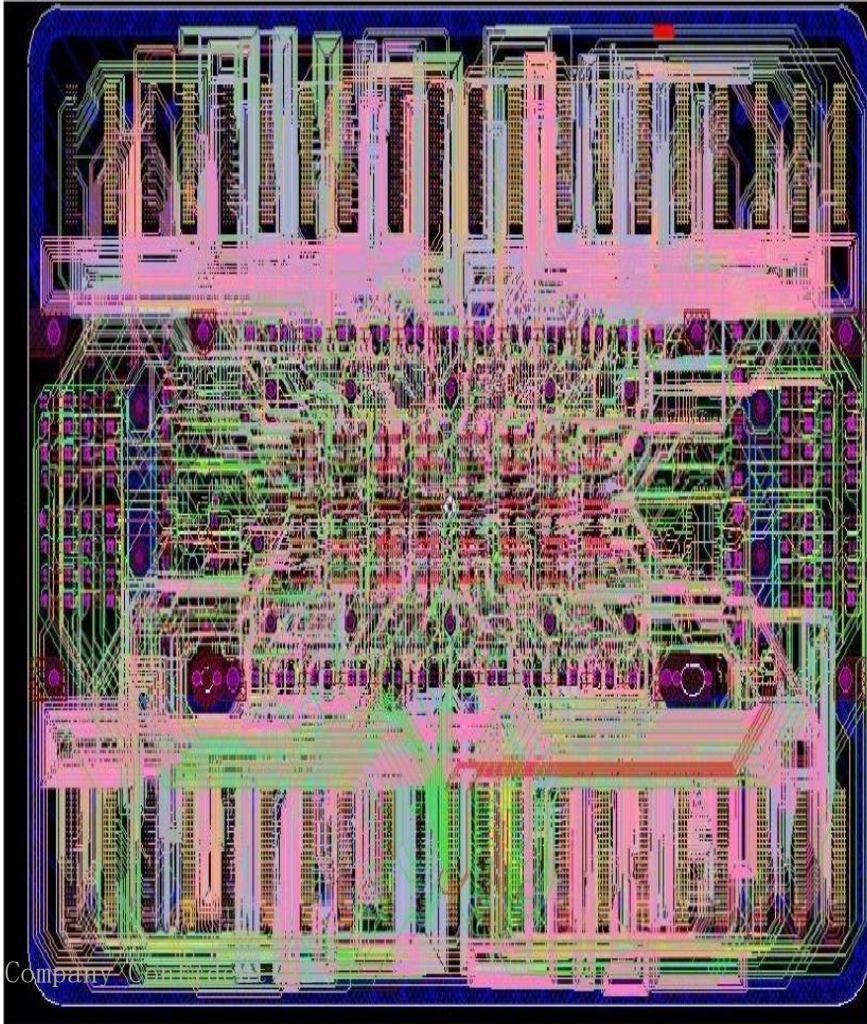
LTX FUSION – LOAD BOARD



- Quad Site, 432 pin BGA
- 1 mm pitch, Mixed Signal Device
- 784 signals
- 50 & 100 Ohm Controlled Impedance
- Delay matching for all signals
- 36 layers
- Material: FR4
- 4.75mm Board Thickness



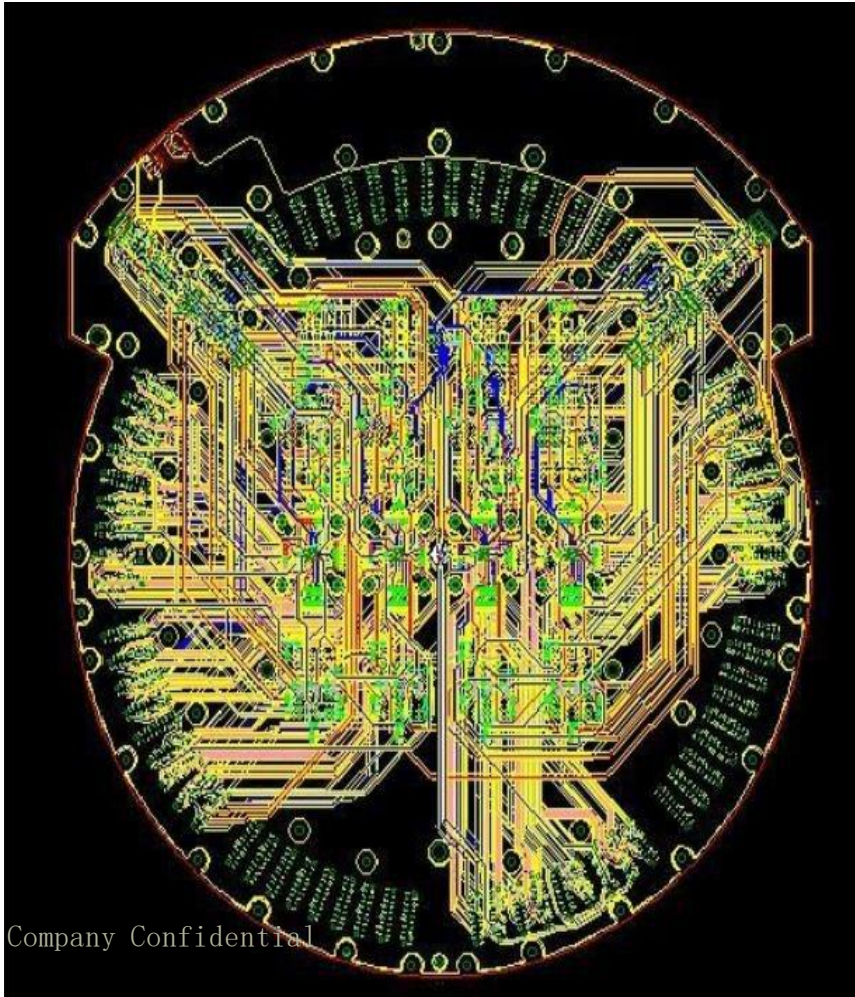
TERADYNE J750 – LOAD BOARD



- 32 Sites, 30 pin SOIC
- 1.27 mm pitch, Mixedsignal
- 804 signals
- 50 & 100 Ohm Controlled Impedance
- Delay matching for all signals
- 966 components
- 38 layers
- Material: FR4
- 5.08mm Board Thickness



TERADYNE CATALYST – LOAD BOARD



- Quad Site, 441 pin BGA
- 0.65 mm pitch, Mixed signal
- 812 signals
- 50 & 100 Ohm Controlled Impedance
- Delay matching for all signals
- 392 Components
- 24 layers
- Material: FR4
- 4.75mm Board Thickness

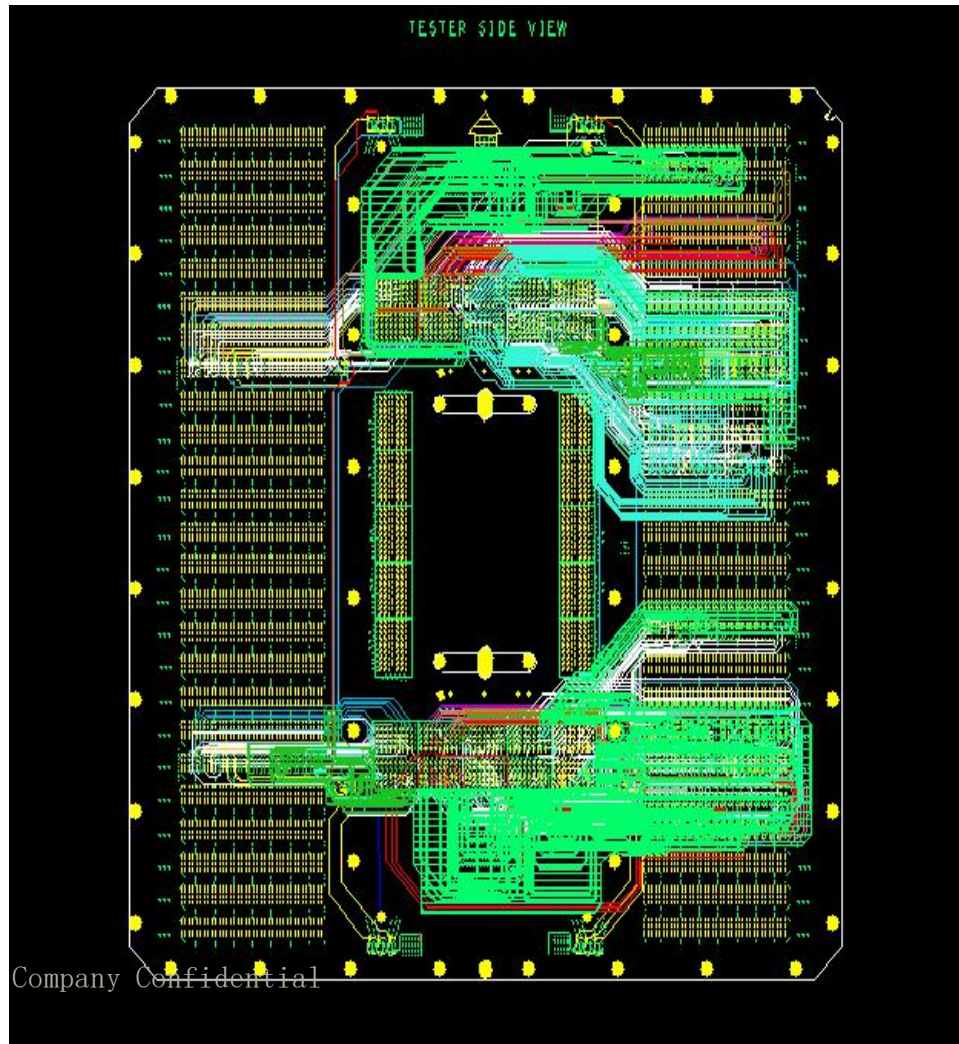


TEST BOARD EXCERPTS

PIB BOARDS



TERADYNE FLEX – PROBE INTERFACE BOARD

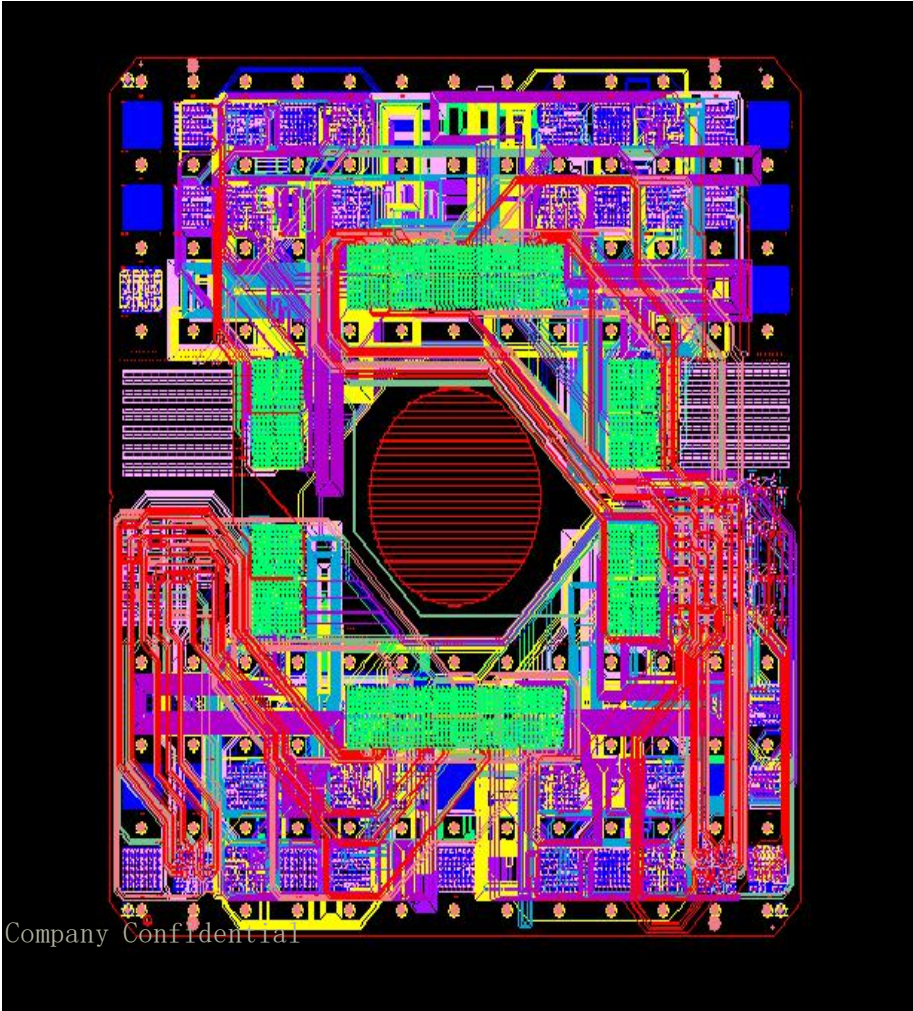


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- 4-HSD200,1-MICROWAVE,1-VHFAC,1-BBAC,1-POOL2 & 1-DC30 Instruments were used
- 128 Utility Signals
- 50 ohm controlled impedance
- POOL2 signals are routed with proper Guarding
- DC30 force & sense traces are routed as Kelvin routing
- 28 layers
- Material: Nelco-4000-7-SI
- 5.08mm Board Thickness



TERADYNE ULTRAFLEX – PROBE INTERFACE BOARD



- 8-Ultrabin800,1-BBAC,2- DC30 & 2-HEXVS Instruments were used
- 1024 signals delay matching within $\pm 0.250''$
- 128 Utility Signals
- 50 ohm controlled impedance
- DC30 force & sense traces are routed as Kelvin routing
- Separate Force & return planes for HEXVS Powers with 2 Oz copper thickness
- 32 layers
- Material: Nelco-4000-13-SI
- 4.75mm Board Thickness

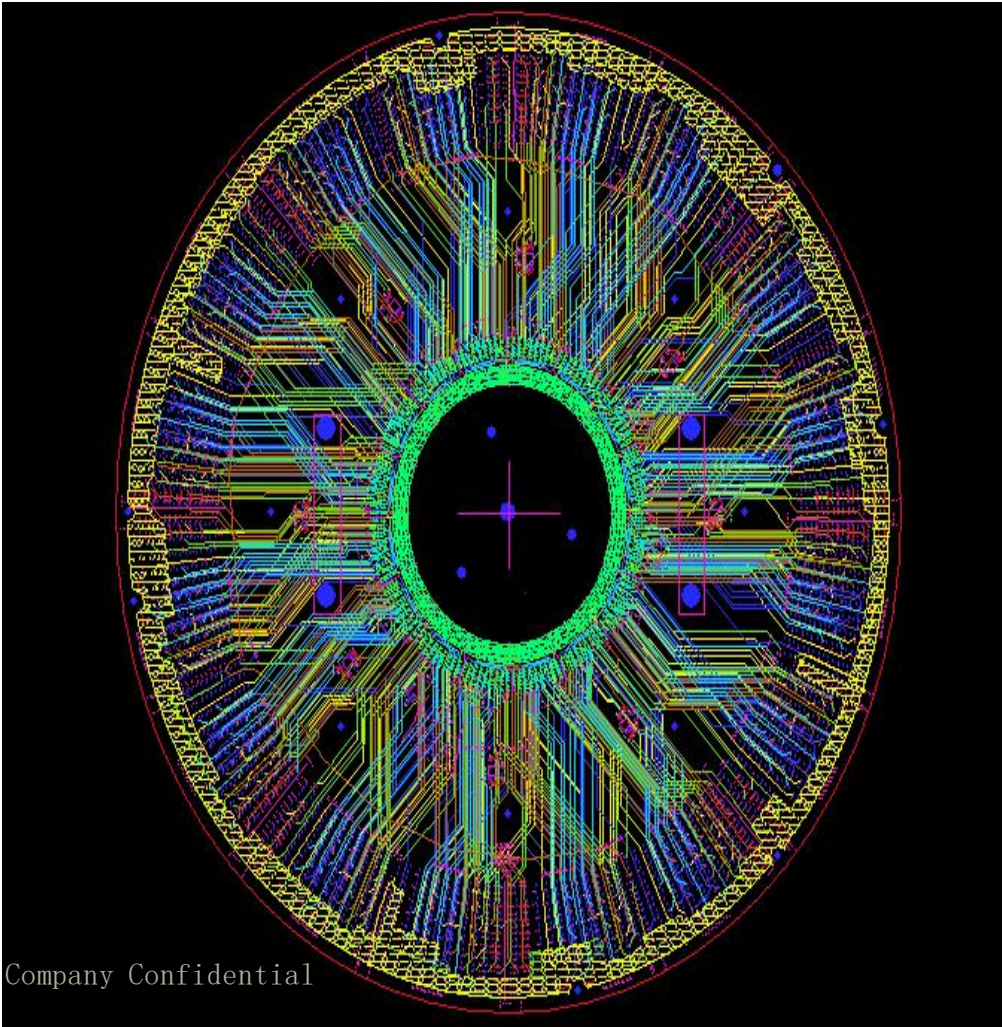


TEST BOARD EXCERPTS

PROBE CARD



TERADYNE J750 – PROBE CARD

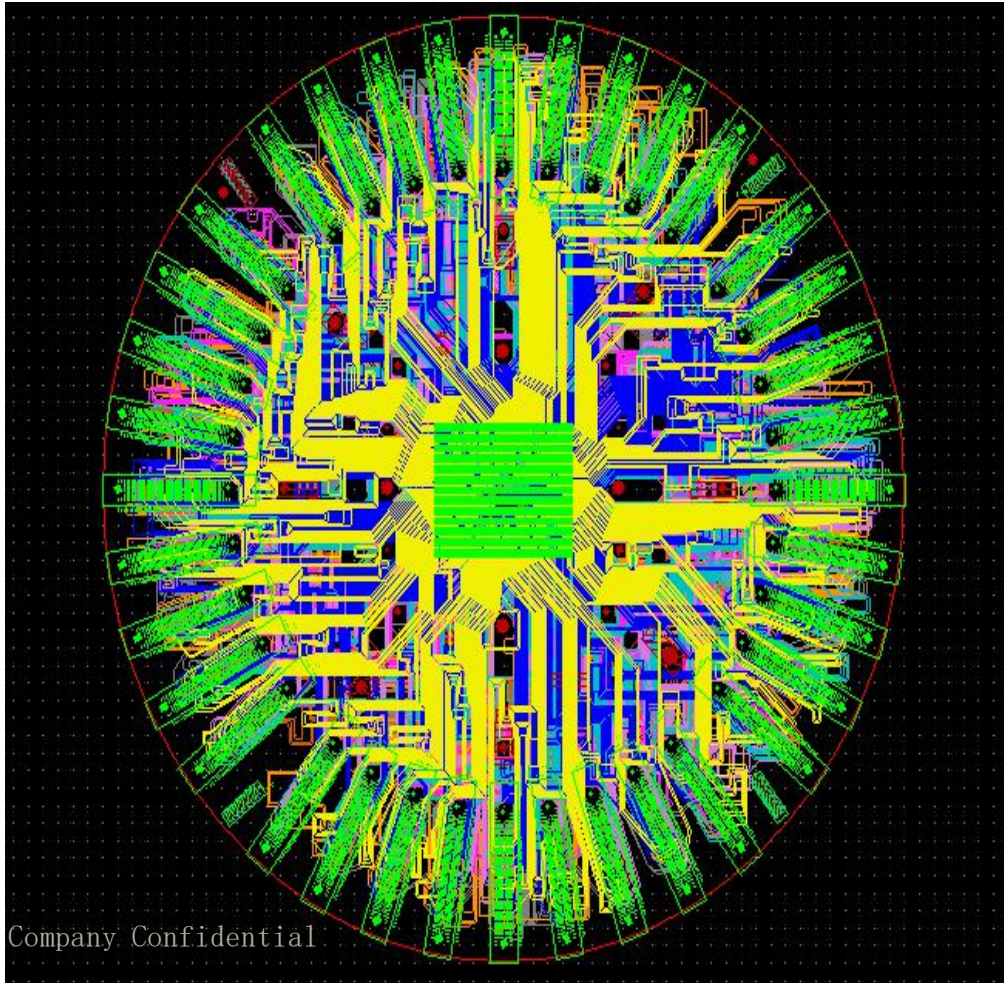


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- Vertical cobra probe card
- 49 pin WLCSP
- 16 Sites
- 784 channels
- 50 ohm controlled impedance
- 64 powers
- 512 components
- 24 layers
- Material: FR4
- 6.35mm Board Thickness



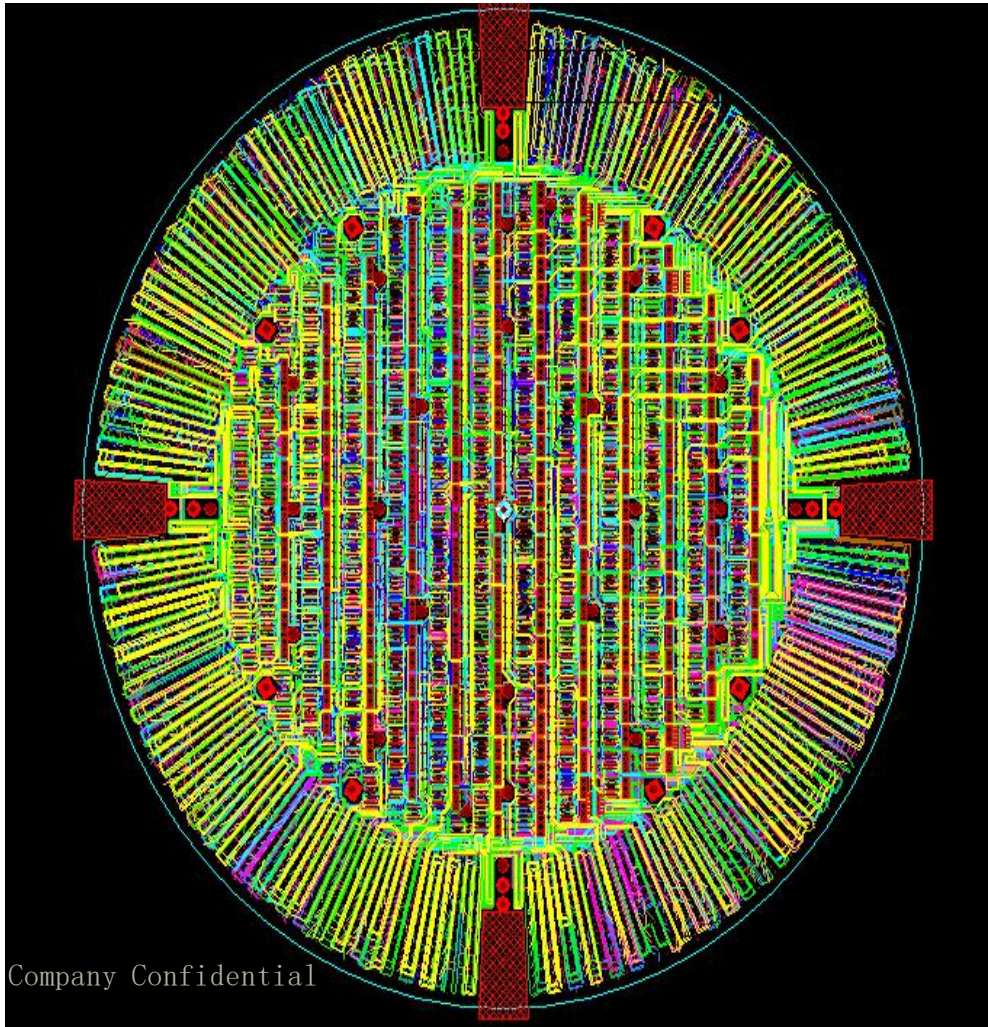
VERIGY5400 – PROBE ARD



- Vertical probe card
- 36 pins\Die
- 143 Sites(11X13 Grid)
- 3575 Signals
- 50 ohm controlled impedance
- Delay matching for all signals
- 286 powers segmentation in 6 layers
- 44 layers
- Material: Polyimide
- 6.35mm Board Thickness



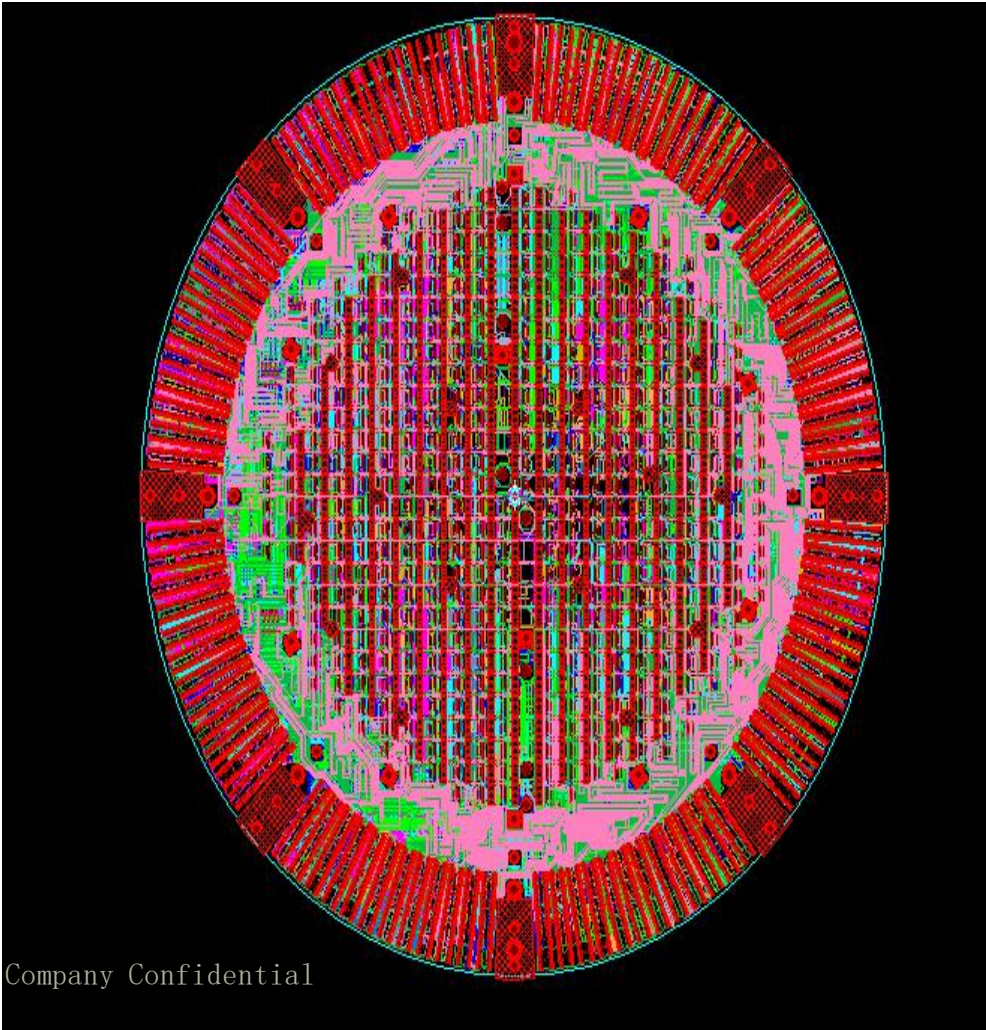
FOS8000 – PROBE CARD



- Vertical probe card
- 18 pins\Die
- 556 Sites
- 1472 Signals
- 50 ohm controlled impedance
- Delay matching for all signals
- 556 powers segmentation in 16 layers
- 56 layers
- Material:Fr4
- 6.35mm Board Thickness



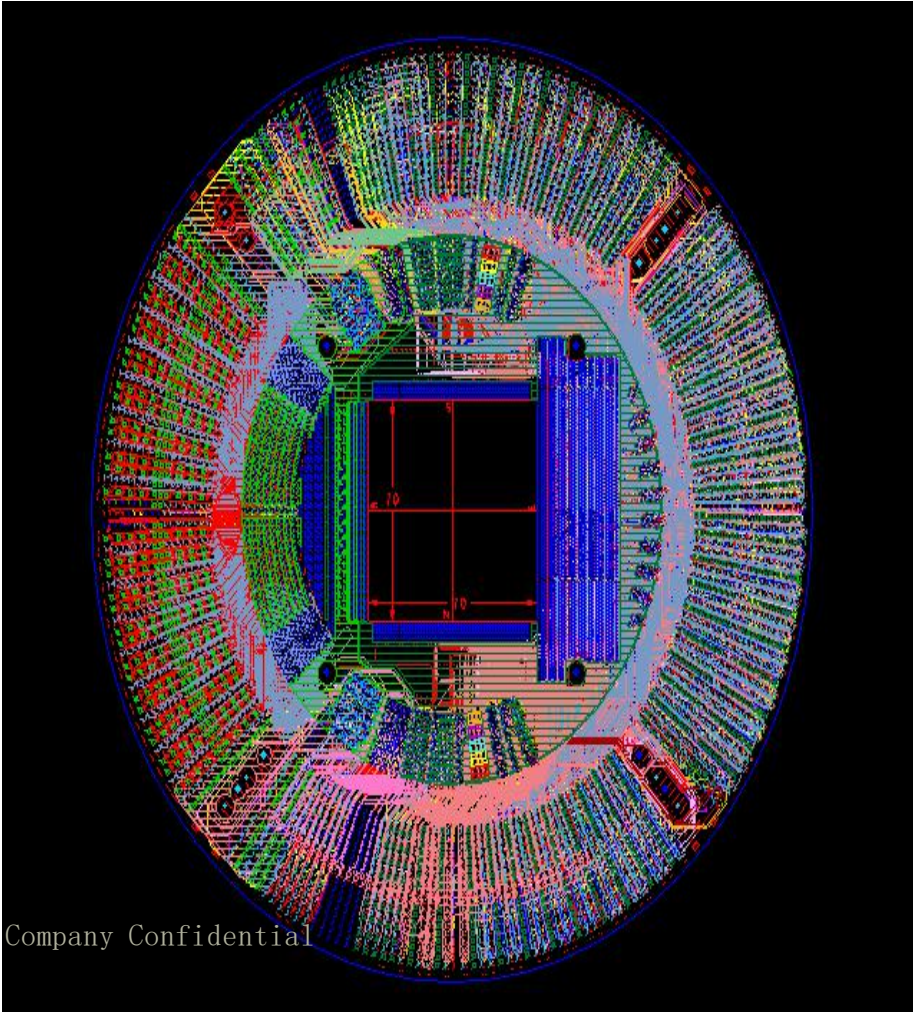
ADVANTEST 5377 – PROBE CARD



- Vertical probe card
- 24 pins\Die
- 432 Sites
- 3698 Signals
- 50 ohm controlled impedance
- Delay matching for all signals
- 432 powers segmentation in 12 layers
- 56 layers
- Material:Fr4
- 6.35mm Board Thickness



ADVANTEST T6373 – PROBE CARD

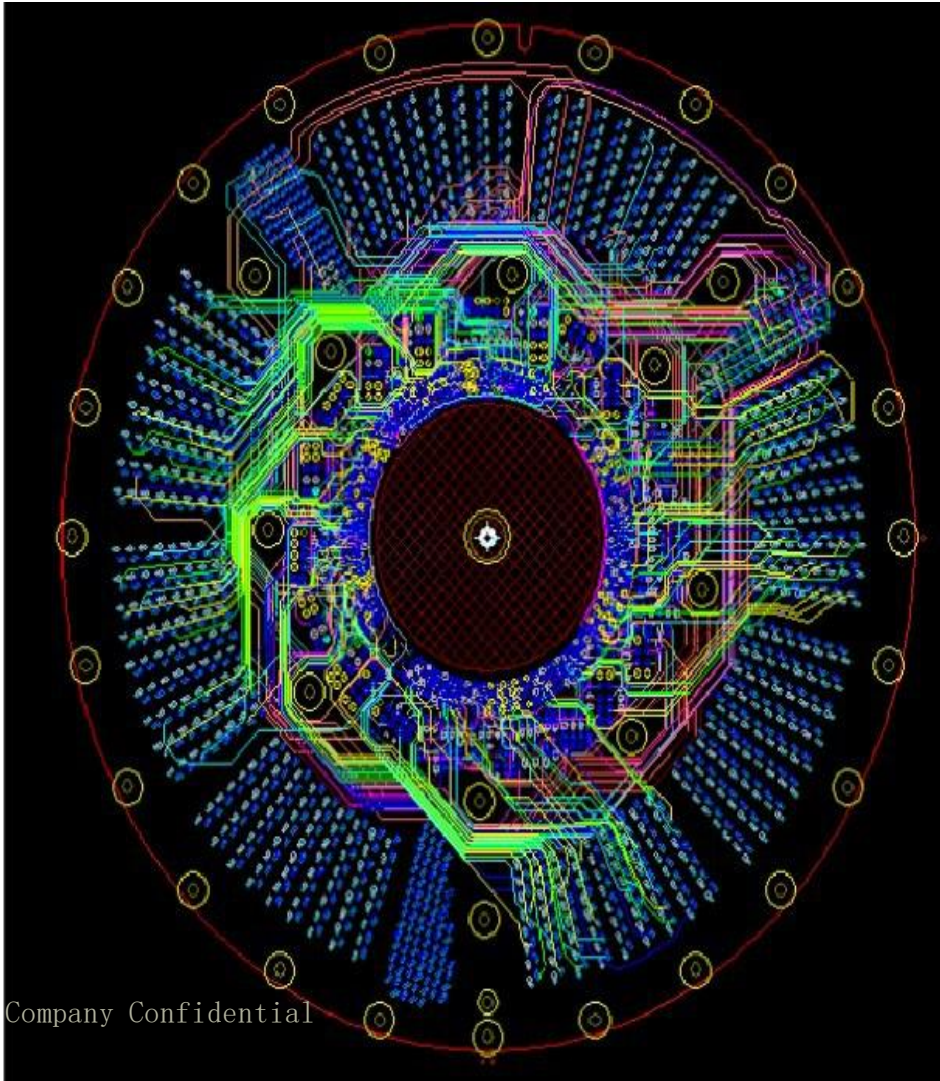


Company Confidential

- Universal Cantilever
- Probe card
 - 2092 signals
 - 128 differential pairs
 - 50 ohm & 100 controlled impedance
 - Delay matching for all signals
 - Diff pair length matching +/-1mils
 - Dual stripline layer configuration
 - 32 layers
 - Material: HI TEMP FR4
 - 6.35mm Board Thickness



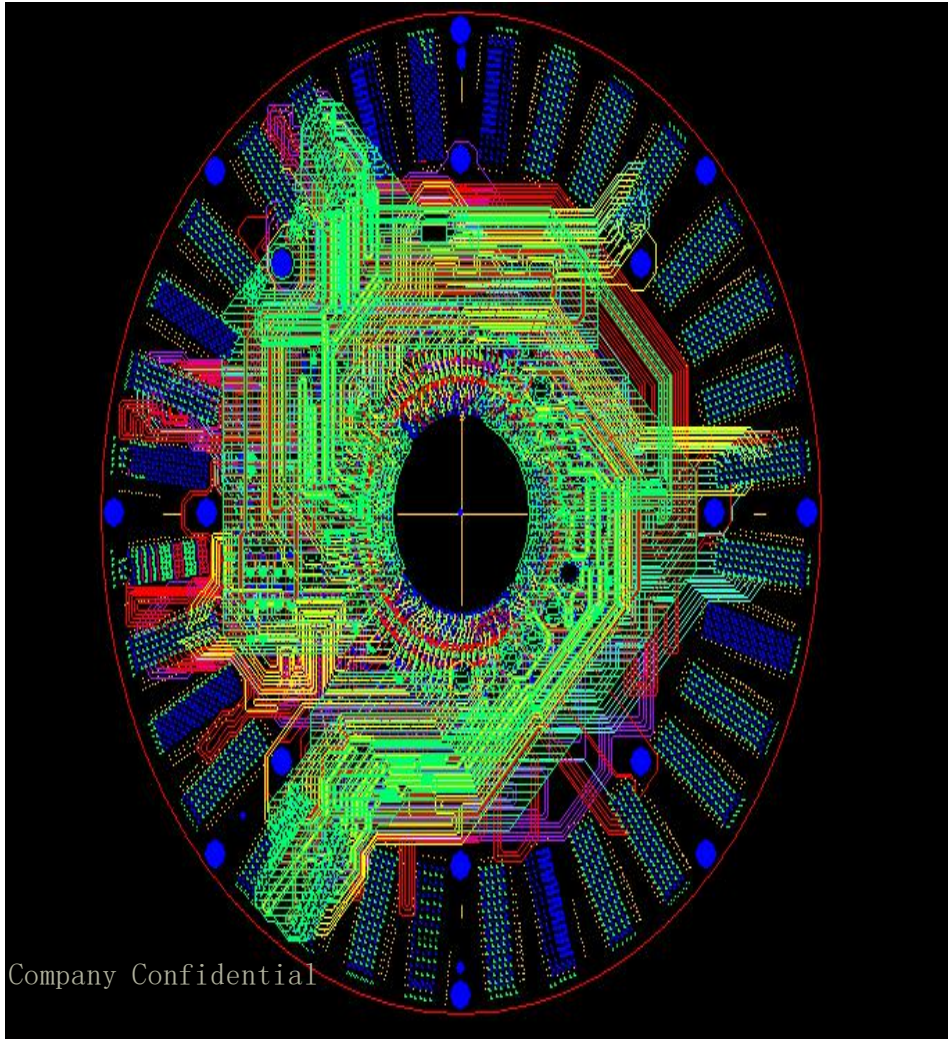
TERADYNE CATALYST – PROBE CARD



- Cantilever Probe card
- 660 signals
- 50 ohm & 100 controlled impedance
- Delay matching for all signals
- Diff pair length matching +/-5mils
- Trace shielding for all diff pairs
- 28 layers
- Material:Fr4
- 4.75mm Board Thickness



CREDENCE SAPPHIRE – ROBE CARD



- Cantilever Probe card
- 976 signals
- 50 ohm & 100 controlled impedance
- Delay matching for all signals
- Diff pair length matching +/-5mils
- Shape shielding for all diff pairs
- 22 layers
- 5mm Board Thickness



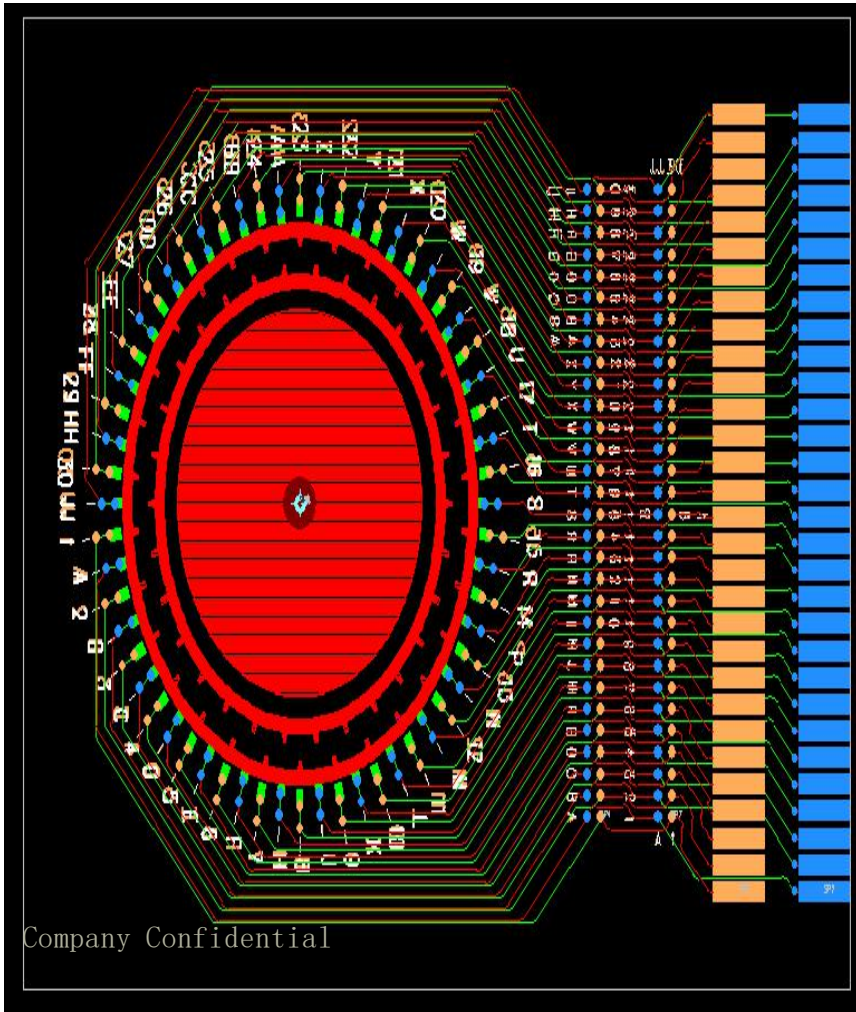
CUSTOMIZED PROBE CARDS



- 256 Probe lands
- 4 layer board
- Material: HI TEMP FR4/Polymide
- High temperature & Cold Probing
- 1.6mm Board Thickness



CUSTOMIZED PROBE CARDS





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Thank You

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