



Caliber Interconnect Solutions

Design for perfection

PCB Design Capabilities



**High Speed & High Density
Interconnect
Design/Analysis/Routing Services**

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Mission & Vision

Mission

“Provide dependable solutions to the satisfaction of the customers through intensive R&D and proven quality control procedures using disciplined workforce.”

Vision

“Developing and applying technological solutions to the benefits of the society that will not affect the safety and living standards of our future generations.”

Quality Policy

“CALIBER INTERCONNECT SOLUTIONS PRIVATE LIMITED is committed to meet and exceed customers expectations through timely delivery of cost effective quality designs through ever improving process and team work.”



Solutions / Services

Embedded

- Turnkey solutions
- Hardware development
- Firmware development

PCB

- HSD
- HDI
- ATE Interface Boards

Simulation

- Signal
- Power
- Thermal

Package

- SiP & multi-chip modules
- Substrate / Interposer (MLC & MLO)
- Both Flipchip & Wirebond

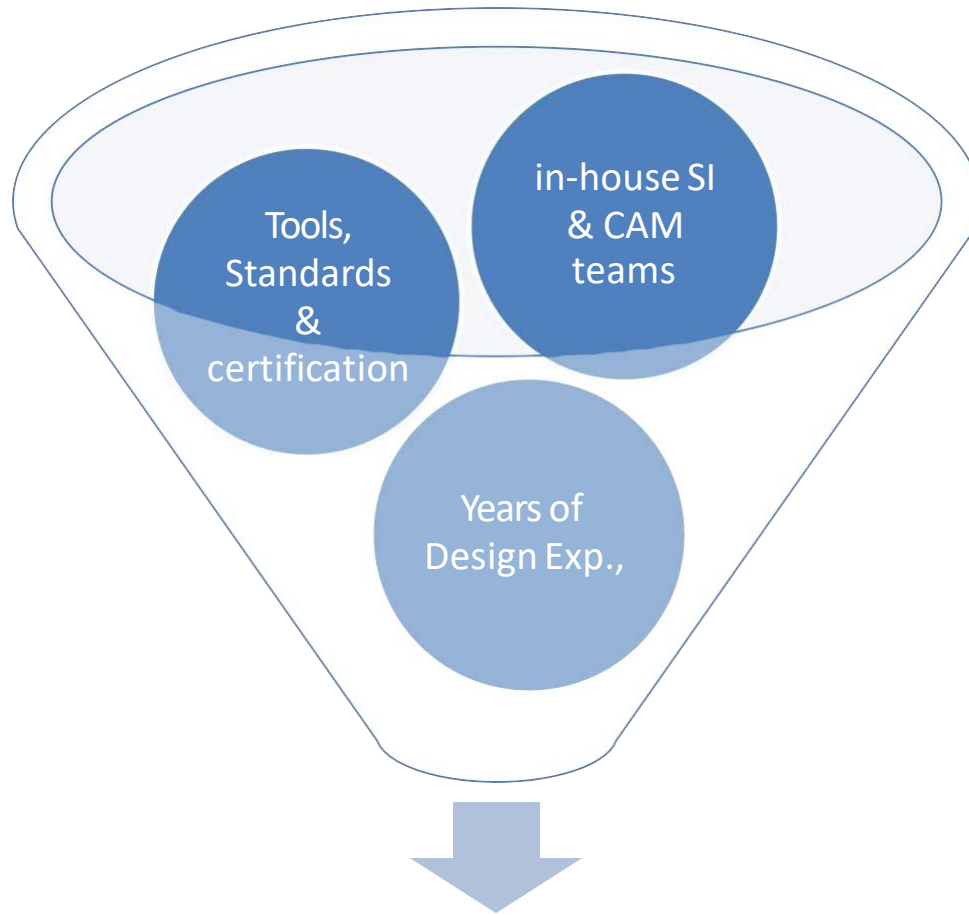


Scope / Theme

- This presentation will help to infer Caliber's PCB design expertise in HSD/HDI variants.
- This doc walks you through relevant sample cases and versatile design summaries.
- Will depict the work flow and approach which we apply to improve our efficacy in HSD/HDI.



Expertise Obtained



HSD / HDI Expertise

Years of design experience combined with the knowledge transferred from in-house Signal Integrity and DFM validation teams helped us to acquire the expertise in HSD & HDI.

Our constant update on EDA/simulation Tools, Standard, training and Certification enables us to deliver for the ever growing industrial needs.



Expertise

Versatile in interfaces and HSD

- :: DDR :: USB :: PCIe ::
- :: SATA :: HDMI :: LVDS ::
- :: SerDes ::
- :: 12~20 Gbps is most common

Fine/HDI DFM handling

- :: 0.4mm pitch BGAs ::
- :: micro via (blind & buried) ::
- :: Hybrid stack-ups ::
- :: Designed max 52 layers in 6.35mm ::
- :: Done 64 layers maximum ::

Design expertise

Electrical knowledge

- :: Mixed signal ::
- :: Mixed impedance design (50/90/100) ::
- :: Mixed topology (Star , chain, tree ...) ::
- :: Skilful in Shield/Tuning/pairrouting ::

Experience

- :: 15 years in PCB design ::
- :: Delivered 7500+ designs ::
- :: Multiple EDA tool knowledge ::
- :: auto-tools and skills for speedy layout ::



High Speed Design consideration

- **Controlled Impedance**
 - Traces
 - VIAS (coupled vias)
 - Component pads
 - Placement optimization (short & straight paths)
- **Material Selection**
 - Loss tangent / dissipation factor
 - Dielectric constant
- **Decoupling**
 - Optimized De-Cap placement
 - Perfect power rail design with low impedance (Z_{11})
 - Capacitor profile selection based on frequency
- **Insertion loss & Skin effect**
 - Length reduction/fixing
 - Perfect tuning for match groups
 - Trace width vs Self inductance
- **EMI & Crosstalk**
 - Ground separation
 - Shielding (with VIAstitching)
 - Appropriate trace separation based on frequency (Trace to Copper and Trace to hole/edges)
 - Perfect return path design
- **Antenna removal**
 - Stub less trace topology
 - VIA stub removal (backdrill or 0-stub by using blind/buried vias)

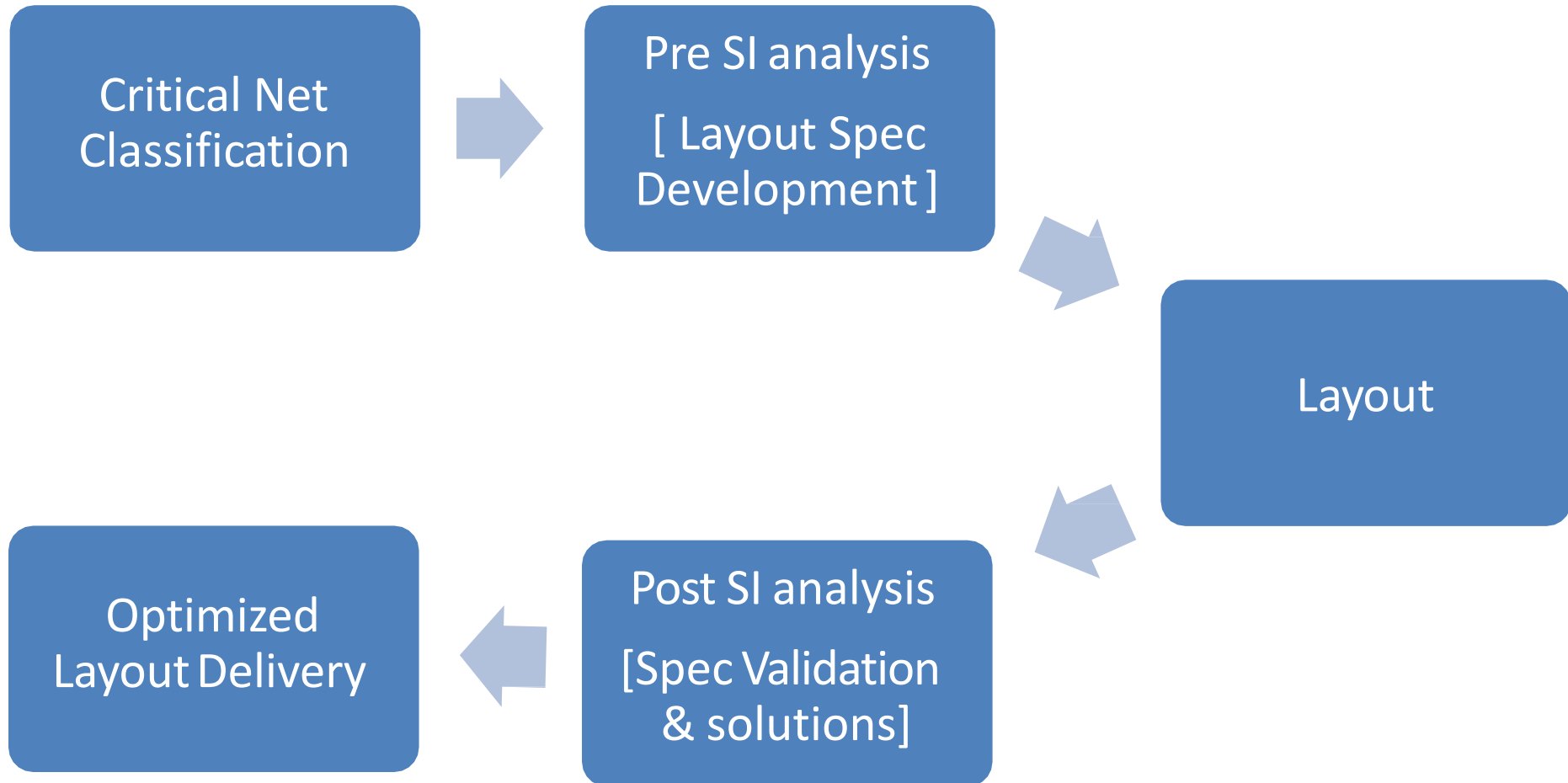


High Density Interconnect

- High Density Placement
- Micro vias (stacked & staggered)
- 1~3 sequential stacks for build-up (on either sides)
- Both Even & Odd layer stacks
- Both POV & Offset vias
- Offset Vias
- Effective handling of Micro, BB and TH in same layout for Cost/Performance optimization
- 0.4mm pitch BGAs
- 0.1mm minimum drill
- Board Thickness ranges from 1.5mm~6.35mm
- Layer count ranges 6~48
- Full HDI (no through hole)
- Hybrid stack-ups
- HSD on HDI



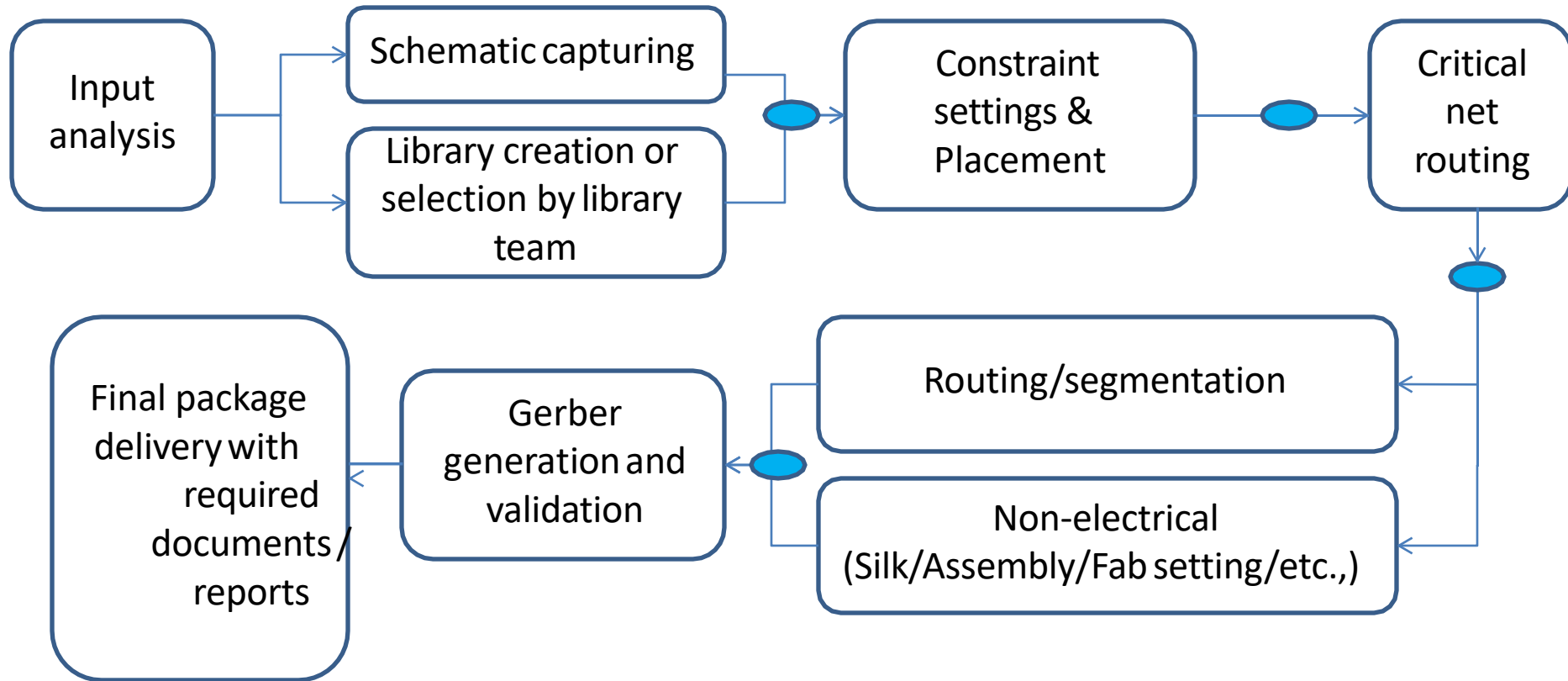
SI + PCB Flow





Layout design flow

The below is the conventional flow of Caliber designs. More opt procedures can be adopted and tailored based on customer needs.



1. Stage-wise review will be done at this points. Also final QA will be done at final stage.
2. After that the files will be sent to customer for review / stage wise approval

Note :

1. Based on customer requirement either entire flow or partial flows can be chosen
2. Layer Stack-up can be discussed & decided based on customer choices and requirements



Samples

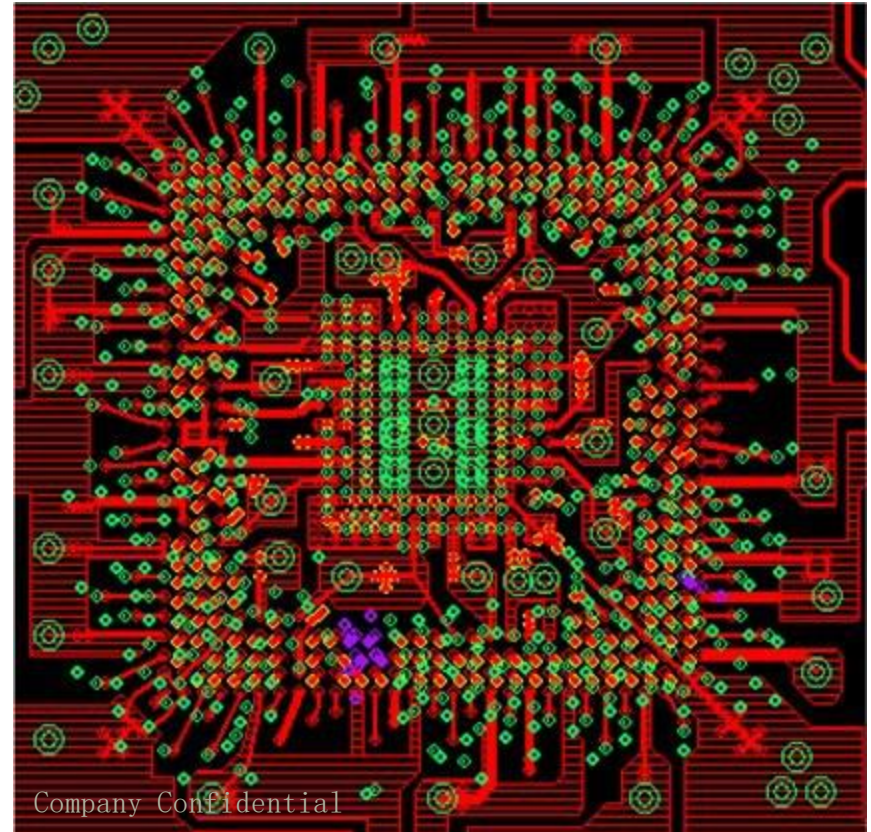
Samples





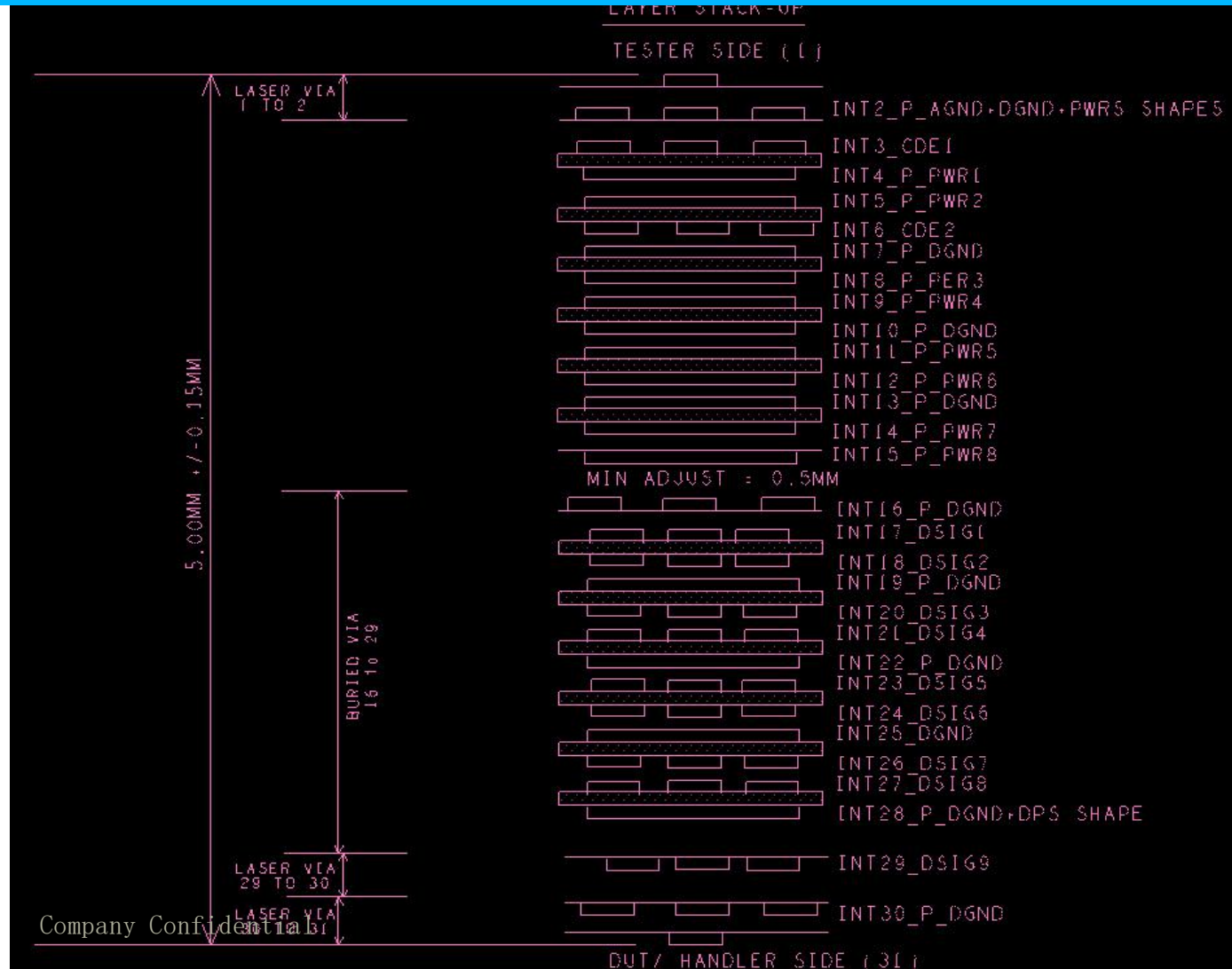
Sample Fanout on 0.4mm BGA

Combination of Micro and BB
vias (Laser & mechanical drill)
for cost Vs performance
optimization on a 6.35mm card



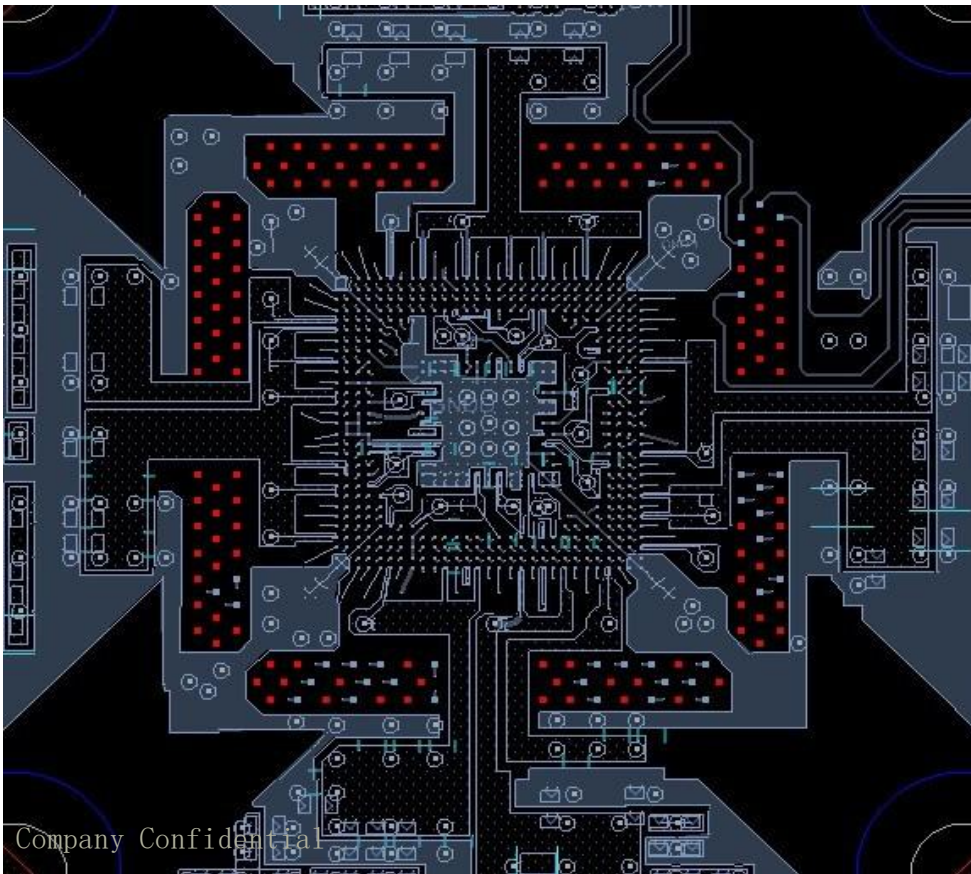


Another Sample Microvia – Stackup (Offset via)





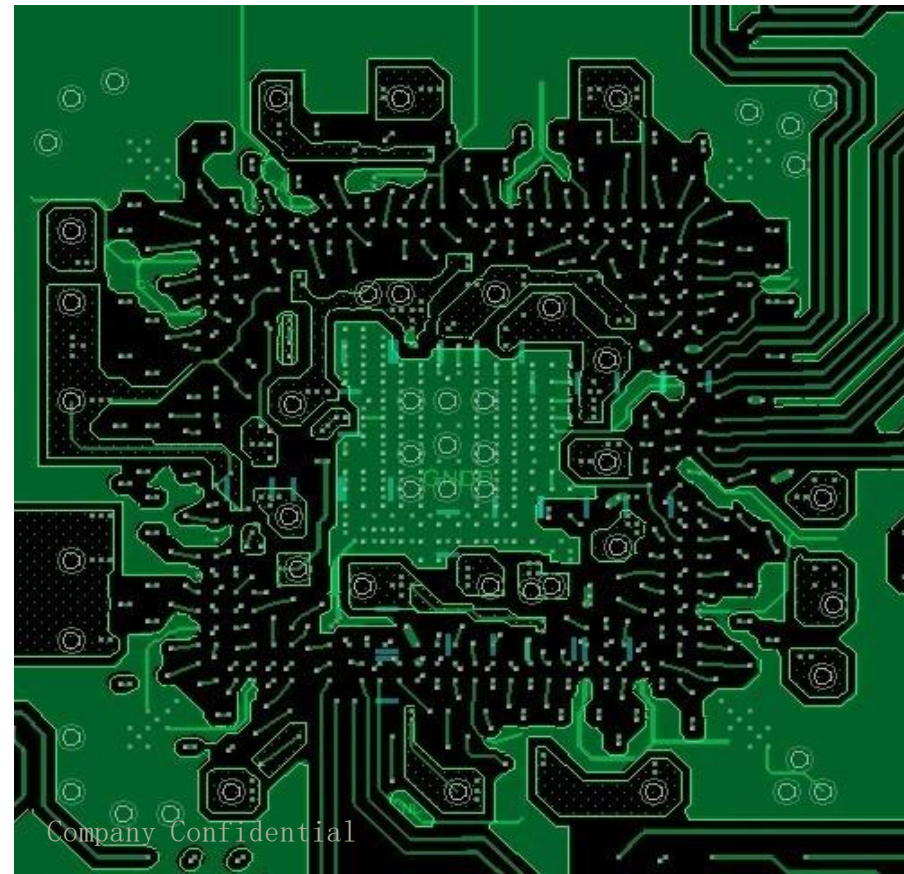
HDI Case : high density region



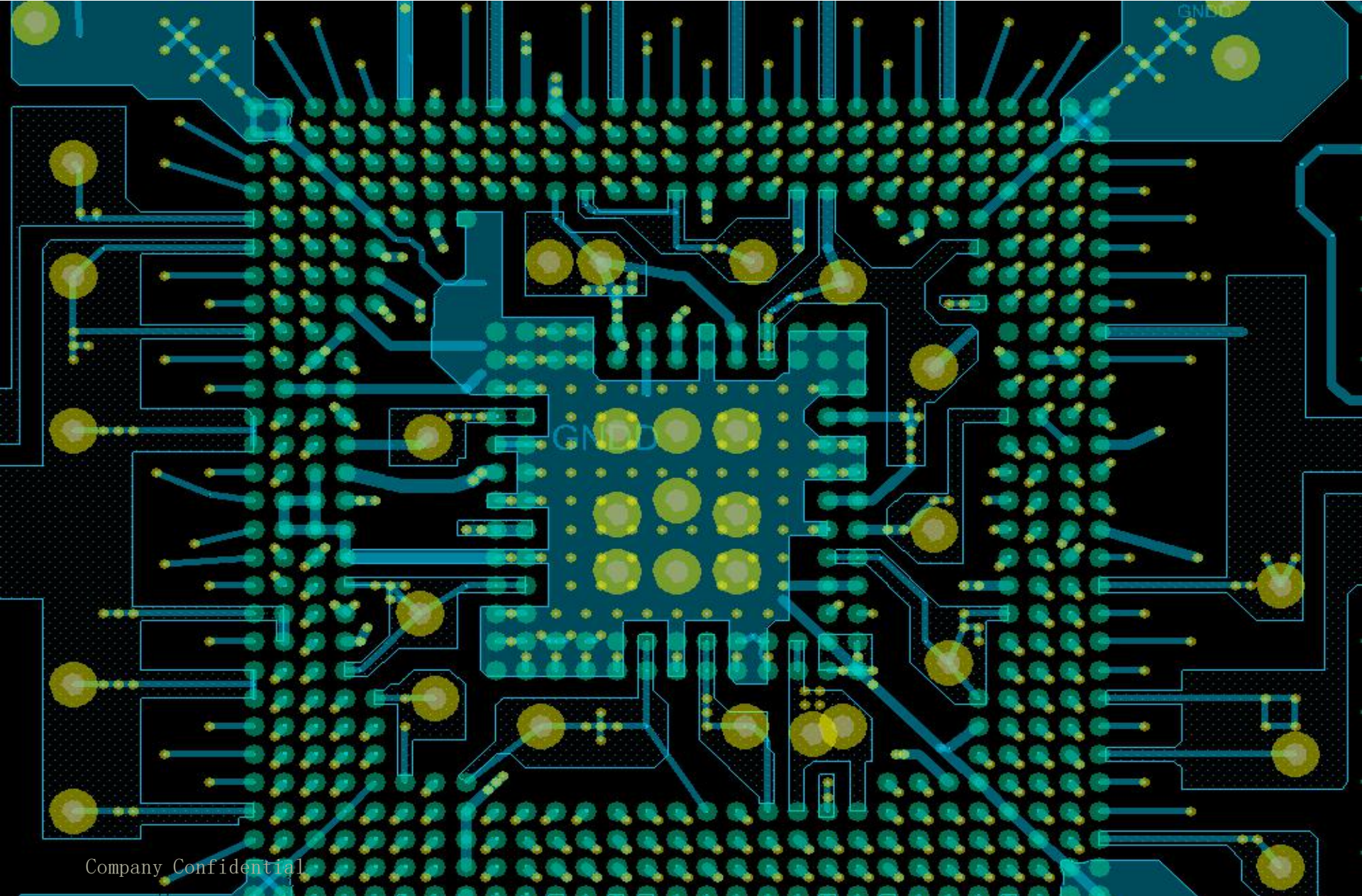
Micro via drill size – 0.1mm

Layer sequences : 30 to 31 & 31 to 32

Staggered Via sequence

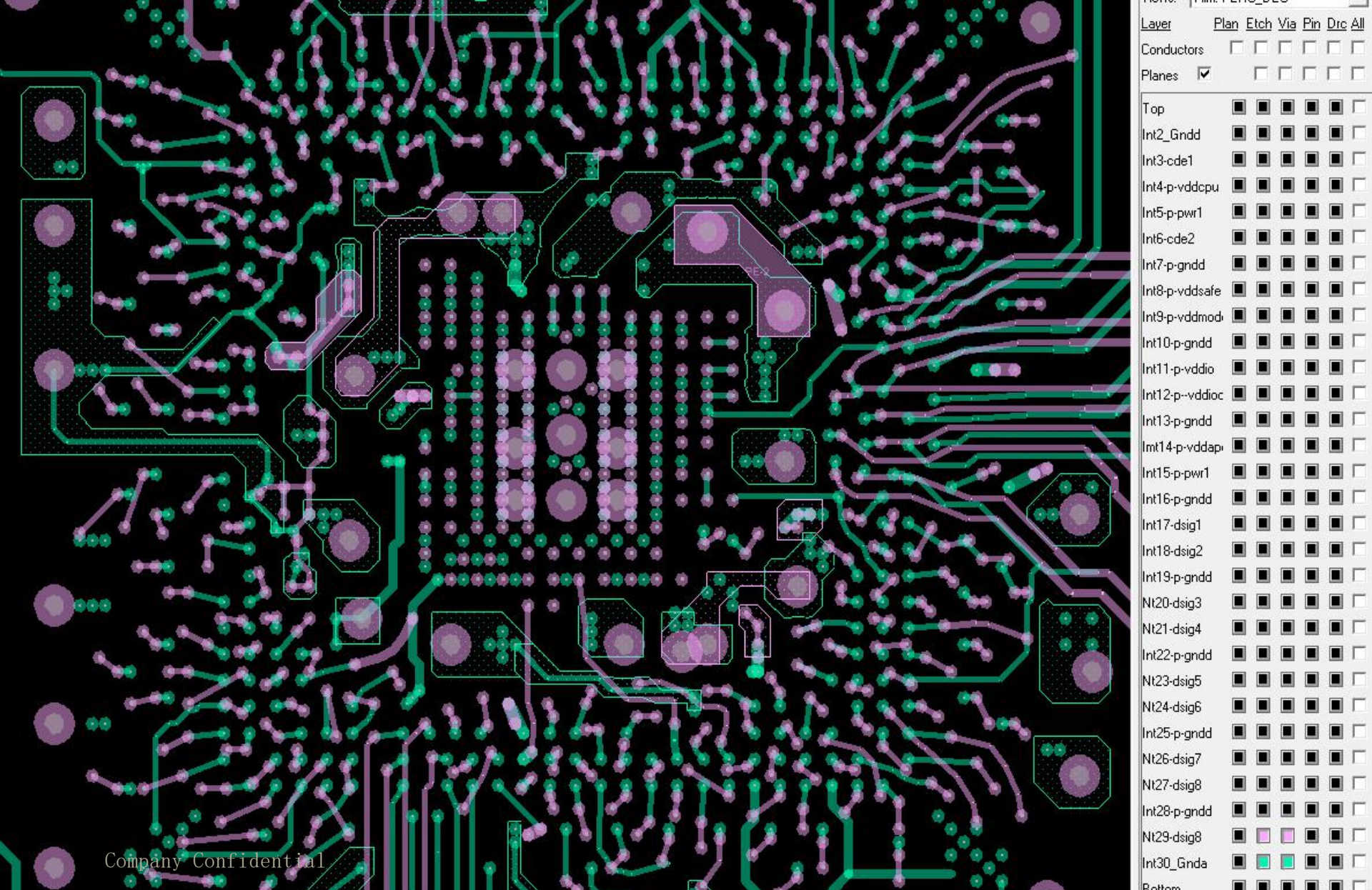


Combination of larger size BB vias used in conjunction with micro vias in order to handle high current rating



Company Confidential

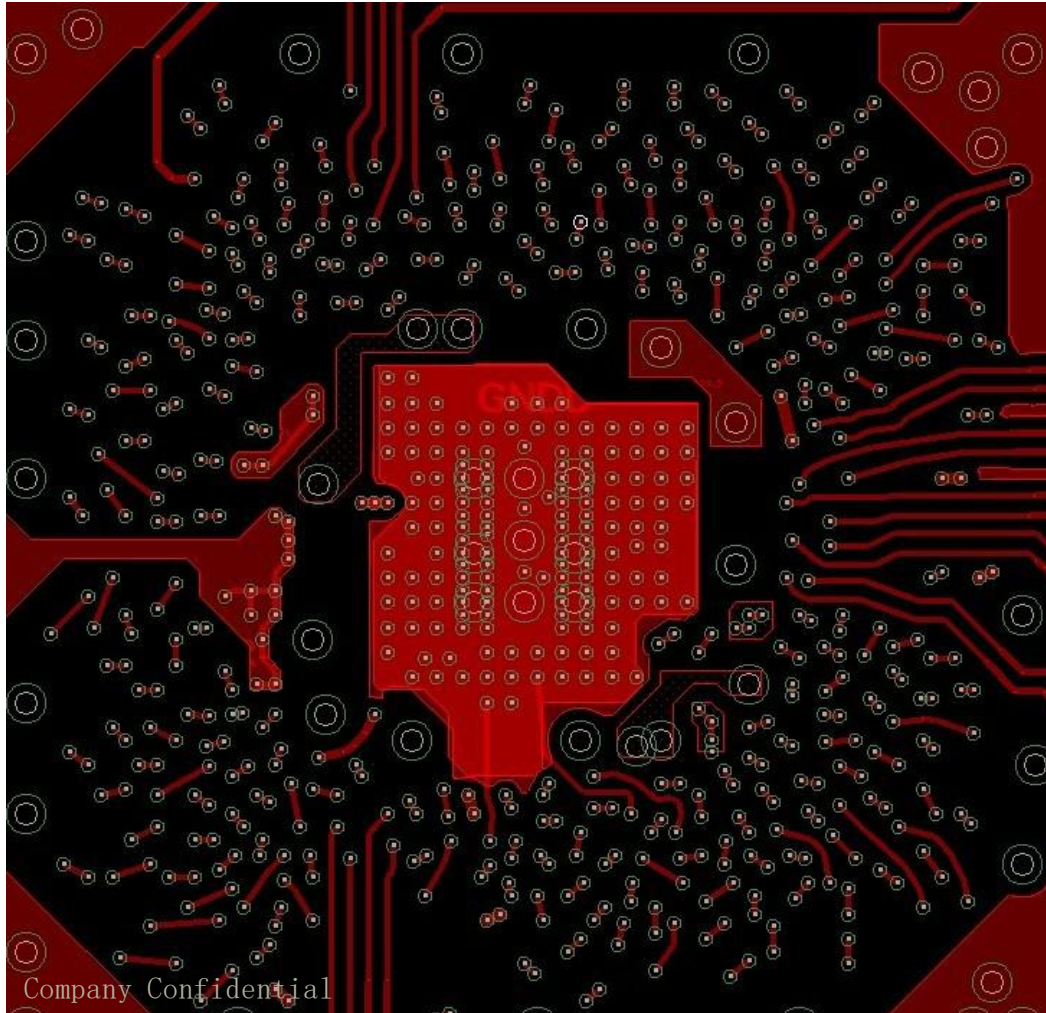
Fanout in Bottom L31 (to L30)



Fanout in L30 to L29



HDI Case : high density region



- Micro vias fanned out to 0.15mm
Buried via structure on L30
- Buried sequence from L17 to L30

Company Confidential



Quick Summaries

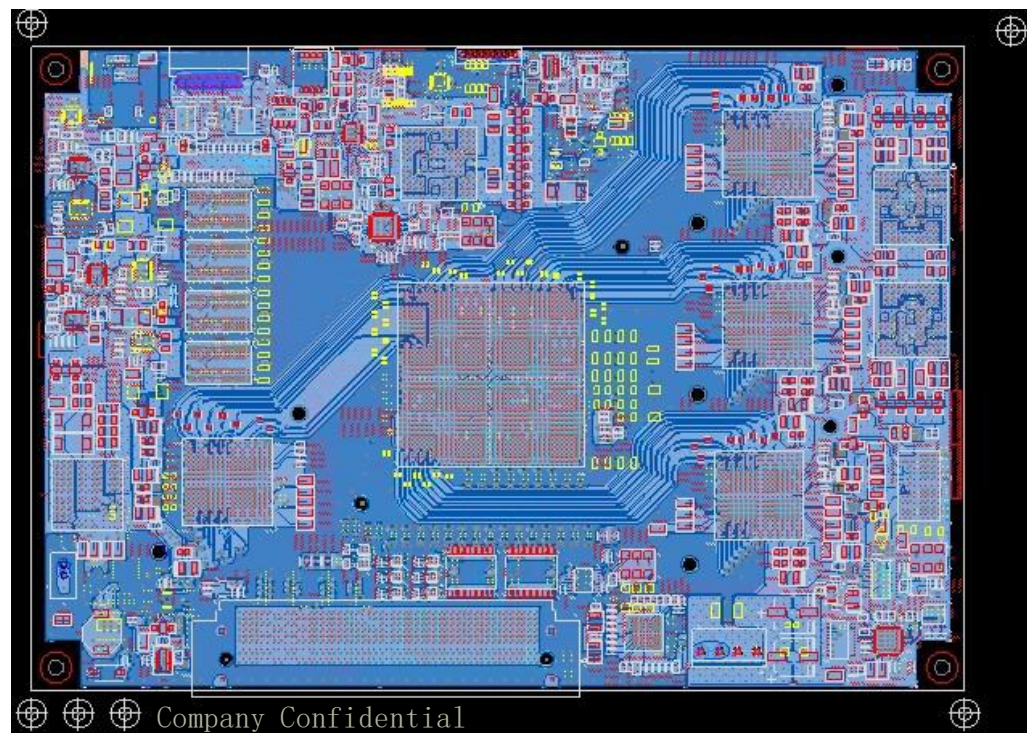
Some more quick summaries





Summary 1 – 8KPROC Board

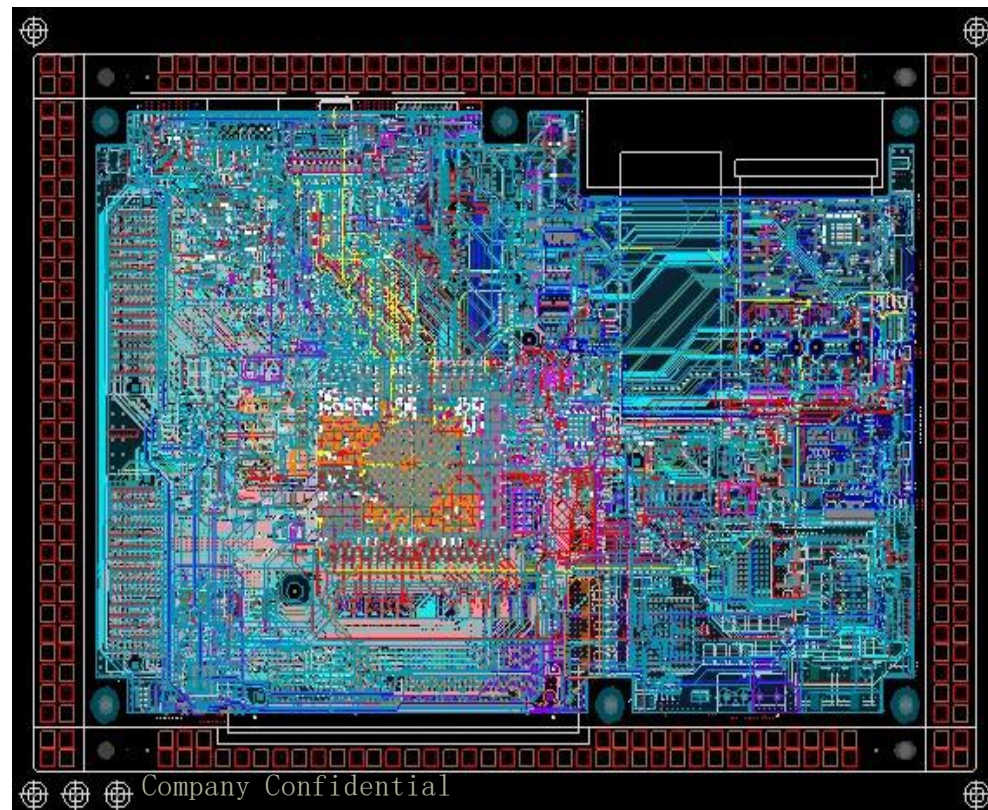
Application : Embedded board
Key Component : Xilinx FPGA processor
Technology : DDR-III, Micro SD , SRAM ,
RS232 , QSPI ,
Backplane Connector,
Frequency : 267 MHz
Data Tran/ Rec speed : 10.692Gbps (backplane conn)
Data Tran/ Rec speed : 12.5Gbps (SRAM)
Board Size : 200X140 MM
Layer Count : 16 Layers
Total Components : 1953
Total No. of pins : 8962
No. Of net's : 1291
No. Of connections : 7172
Design Complexity : 1.00mm pitch 1517 FBGA pins
: 1.00mm Pitch 324 BGA pins (4X SRAM)
: 0.8MM Pitch 96 pins (4X DDR3)
: 1.27MM Pitch 401 pins (backplane Conn)
: 278 diff pair's & used Arc routing for all
Differential pair's signals
EDA Tool Set : Allegro PCB Editor



Summary 2 – OPT100G_CFP4 Board



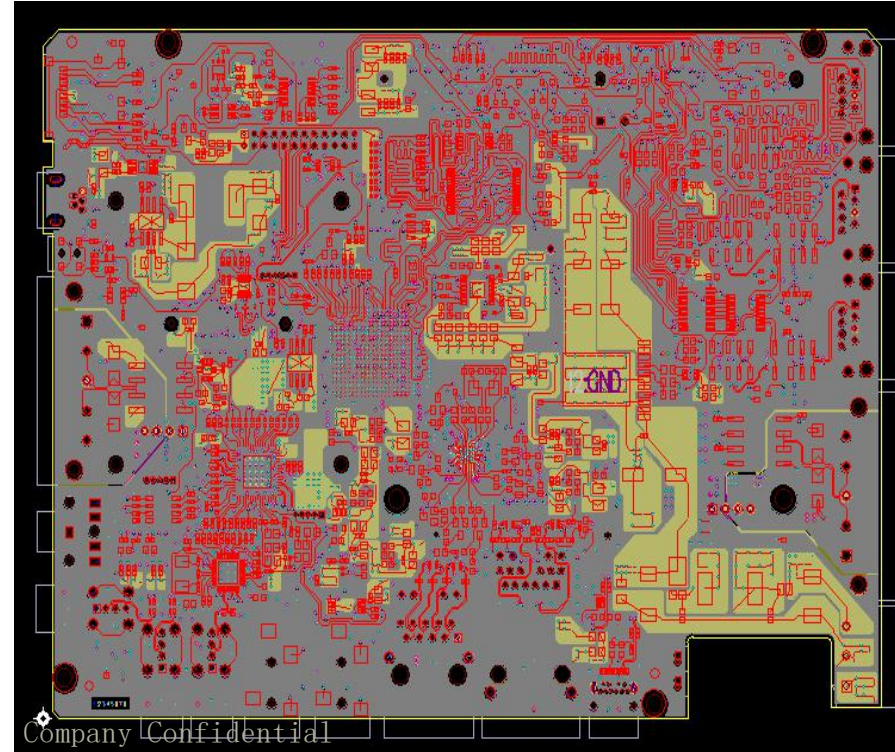
Application : Embedded board
Key Component : Xilinx FPGA processor
Technology : DDR-III, Micro SD,SFP con,
CFP4 con , Firefly, RS232 , QSPI ,
Backplane Connector,
Frequency : 267 MHz
Data Tran/ Rec speed : 10.692Gbps (backplane conn)
Board Size : 200X140 MM
Layer Count : 16 Layers
Total Components : 1408
Total No. of pins : 7626
No . Of net's : 1401
No . Of connections : 5772
Design Complexity : 1.00mm pitch 1924 FBGA pins
: 0.5MM Pitch 40 pins firefly conn
: 0.8MM Pitch 96 pins
: 1.27MM Pitch 401 pins (backplane Conn)
: 1.27MM Pitch 301 pins (2 X backplane Conn)
: 328 diff pair's & used Arc routing for all
Differential pair's signals
: Used 0.25mm blind via
EDA Tool Set : Allegro PCB Editor



Summary 3 – PLC020 Carrier Board Board



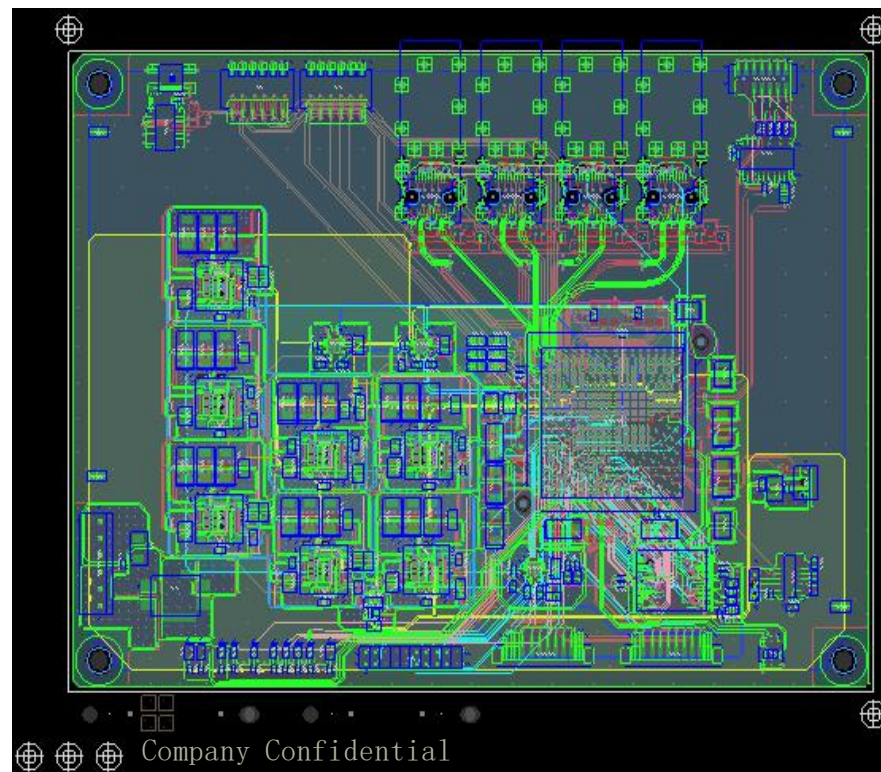
Application	: Embedded board
Key Component	: LATTICE FPGA processor
Technology	: SRAM, EEPROM, Micro SD, CAN con, Rs232, Rs485, LVDS, PCIe USB HUB, USG OTG, Ethernet jack MXM con ,HDMI Display port, Audio Jack.
Frequency	: 200 MHz
Board Size	: 167X118 MM
Layer Count	: 8 Layers
Total Components	: 1220
Total No. of pins	: 4265
No . Of net's	: 817
No . Of connections	: 6002
Design Complexity	: 0.8MM pitch 381 Pins FPGA : 0.4MM Pitch 64 pins BGA : 0.5MM Pitch 64 pins QFN : 0.5MM Pitch 280 pins Board to board con : 0.6MM Pitch 100 pins Board to board con : 0.8MM Pitch 50 pins Board to board con : 51 diff pair's : Used 0.101mm blind via and 0.2032 mm buried Via : Used .1016 trace width/space
EDA Tool Set	: PADS 9.5v (Mentor graphics)





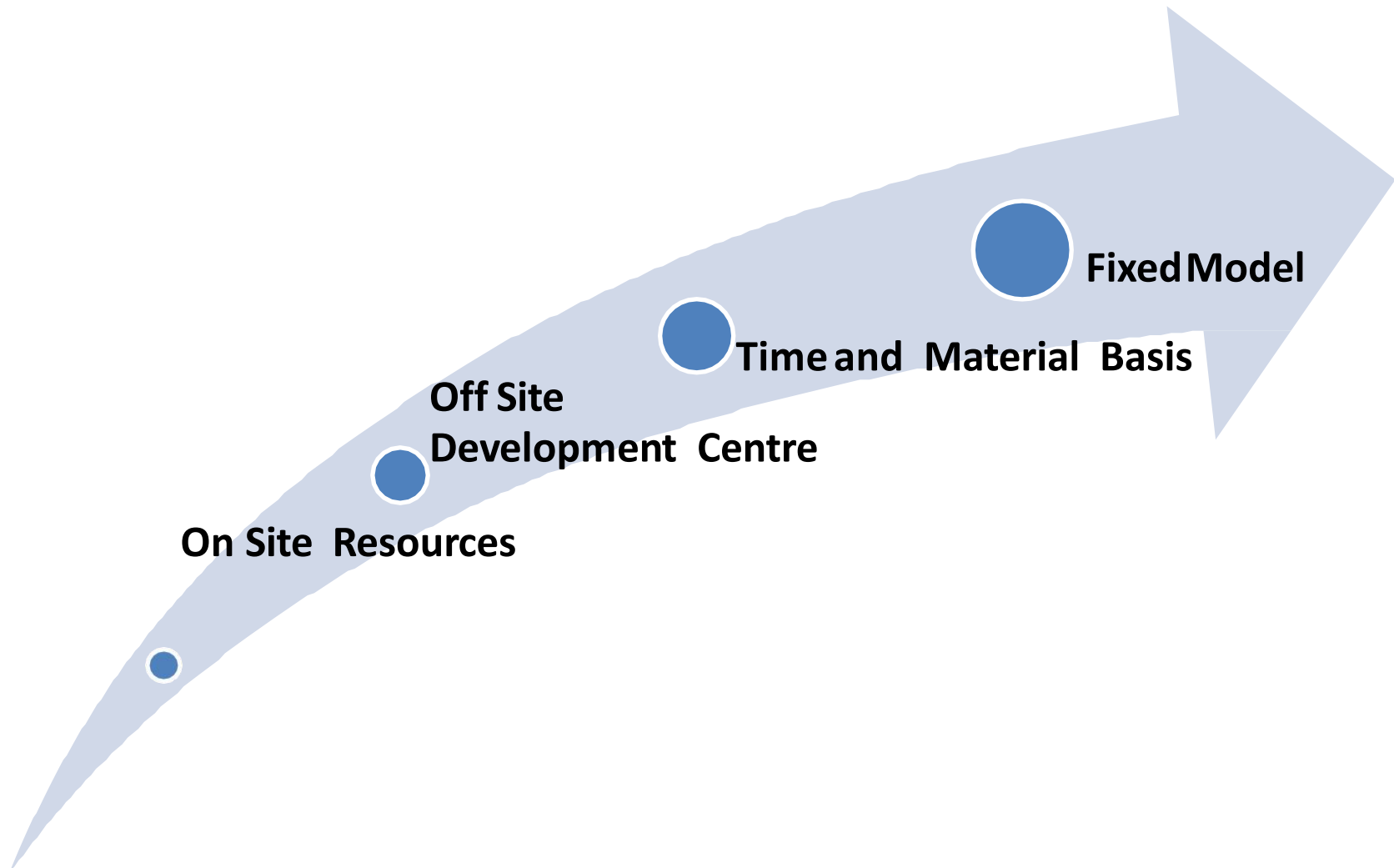
Summary 4 – Medical Board

Application	: Embedded board
Key Component	: XILINX FPGA processor
Technology	: Flash, 4X SFP connector SD,
Frequency	: 312.5 MHz
Data Tran/Rec speed	: 6.6 Gb/s to 28.05 Gb/s
Board Size	: 200X150 MM
Layer Count	: 12 Layers
Total Components	: 380
Total No. of pins	: 2631
No . Of net's	: 277
No . Of connections	: 1832
Design Complexity	: 1.0MM pitch 1157 Pins FPGA : 0.8MM Pitch 22 pins 4 X SFP connector : 13 diff pair's : Used 0.1 mm trace width/Space used Arc routing for all Differential pair's signals
EDA Tool Set	: Allegro PCB Editor





Business models





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Thank You

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